

# Compal Confidential

## Hasswell M/B LA-9313P Schematics Document

### Intel ULV Processor with LPDDR3

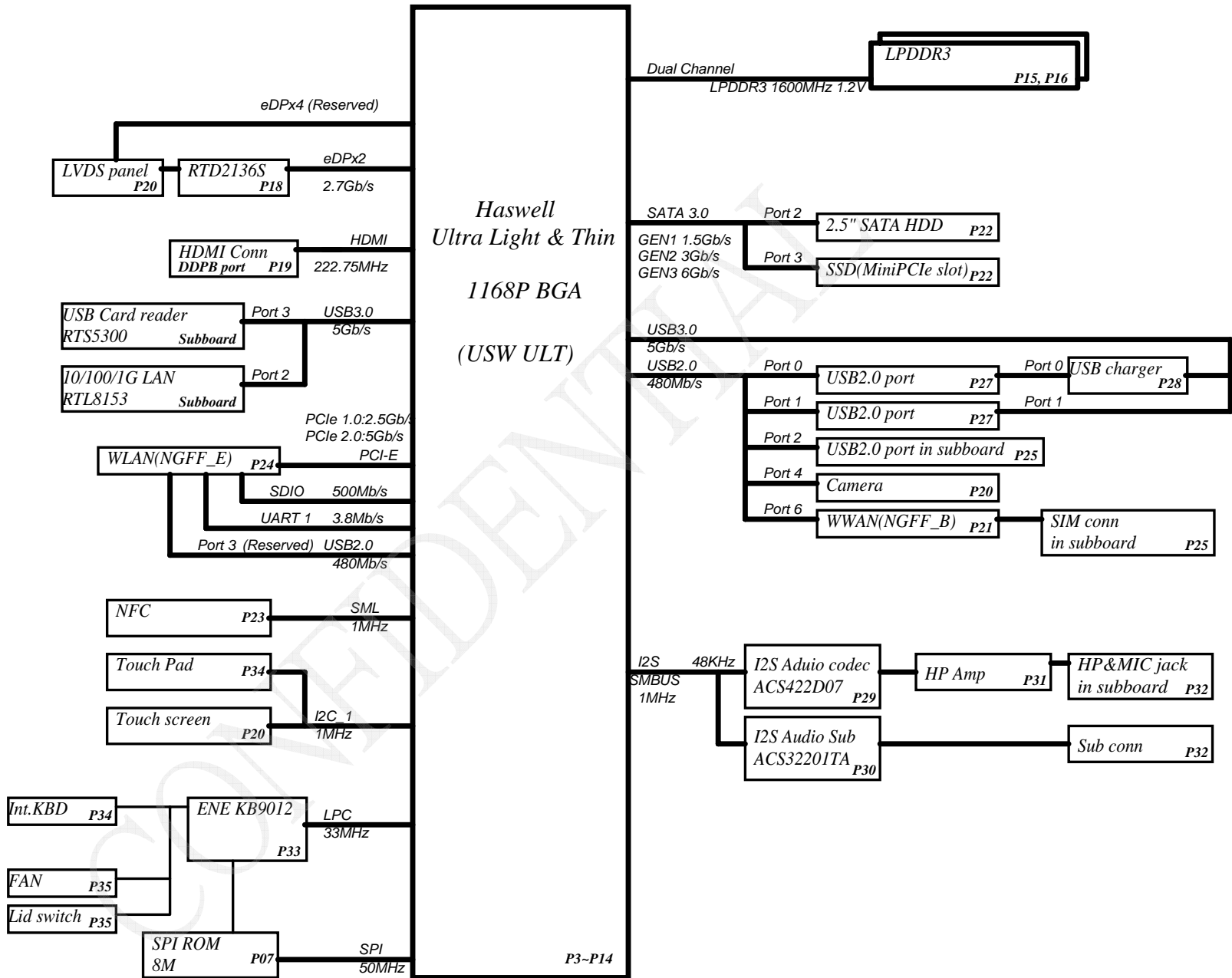
Date : 2013/04/19

Version 0.5

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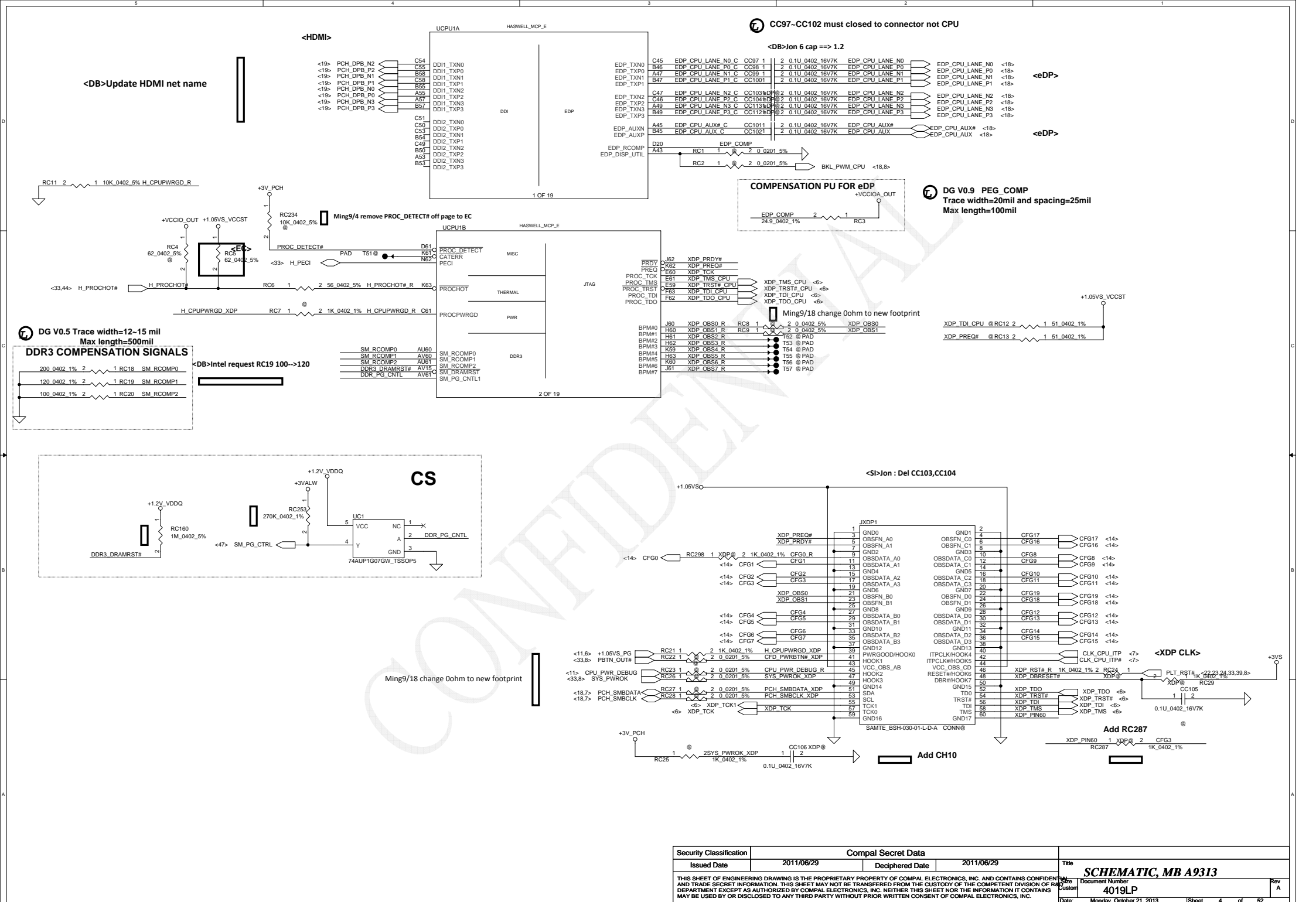
File Name :  
LA-9313PV04

Accelerometer  
HP3DC2 P37

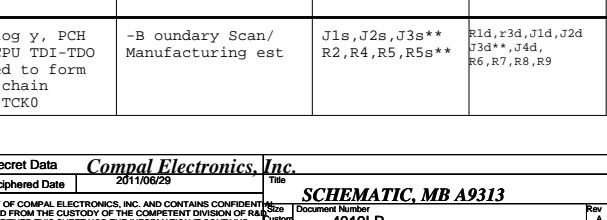
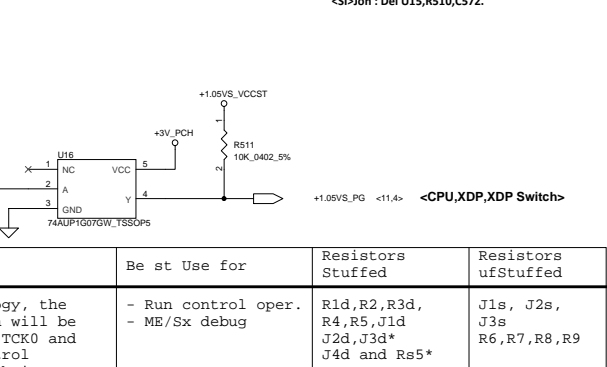
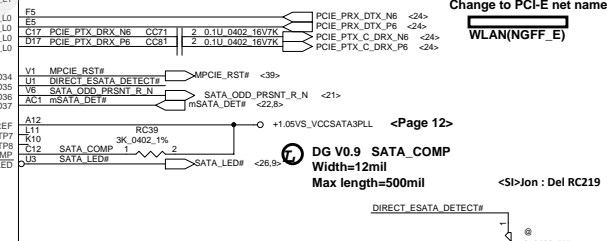
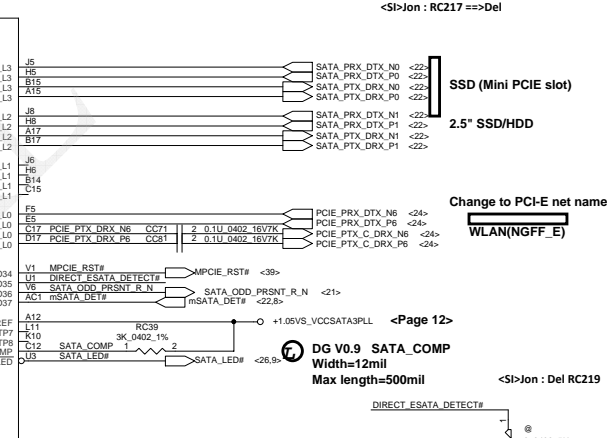
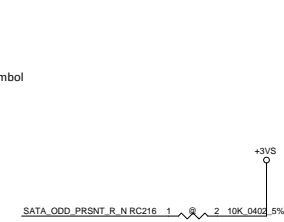


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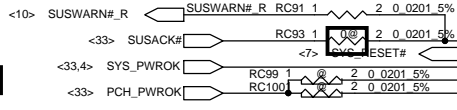


Topolog	Description	Be st Use for	Resistors Stuffed	Resistors u/Stuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topolog y, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s,J2s,J3s** R2,R4,R5,R5s**	R1d,r3d,J1d,J2d J3d**,J4d, R6,R7,R8,R9

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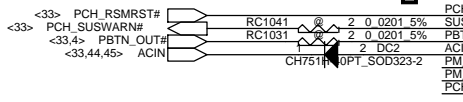


Non Deep S3 RC91-->SMT  
Deep S3 RC93-->SMT



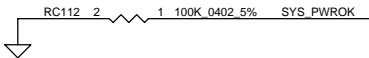
Ming9/18 change 0ohm to new footprint

Deep S3

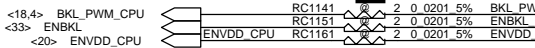


Ming9/13 remove PCH\_SLP\_WLAN#/PM\_BATLOW#  
for BIOS request

<DB>RC112 10K-->100K

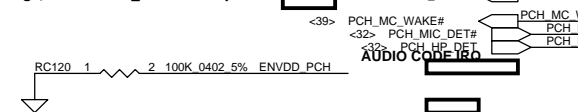


PANEL\_BKEN\_CPU PD 100K on Page20  
Ming9/18 change 0ohm to new footprint

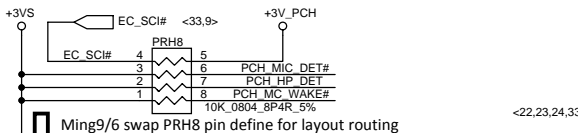


Ming9/12 change EC\_SMI# for BIOS request

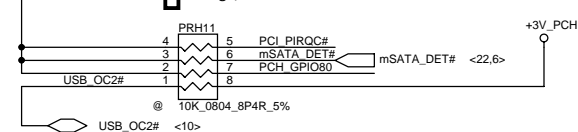
<SI>Jon :change ACCEL\_INT# to GPIO46.  
Ming9/3 removeTP\_res for co-lay eDP



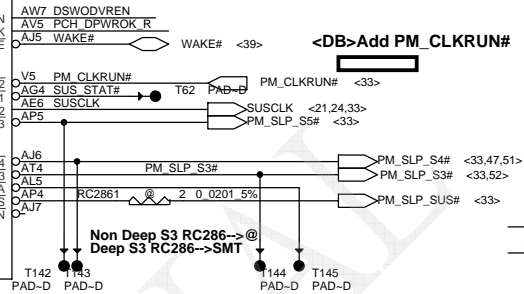
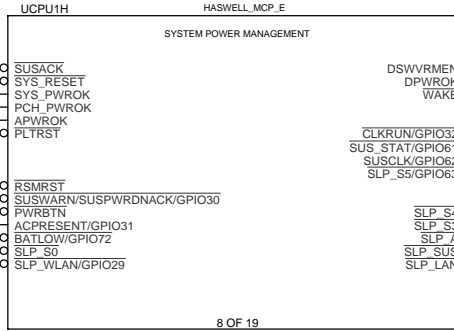
Ming9/12 change PCH\_MIC\_DET#/PCH\_HP\_DET# to GPIO 51/53 for BIOS request



Ming9/17 add RC130 for G-sensor PH

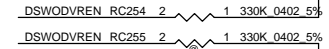


<25,26,33,46> PM\_SLP\_S0# RC268 1 2 0 0201 5% PM\_SLP\_S0# R RC268 or RC269 one mounted.  
<SI>Jon : Change to PM\_SLP\_CS#.



DSWODVREN - On Die DSW VR Enable

\* H : Enable  
L : Disable



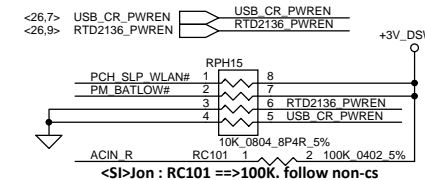
<SI>Jon : RC102 ==>R-Pak RPH14.

<DB>RC106 10K-->100K

<SI>Jon : RC106 ==>10K

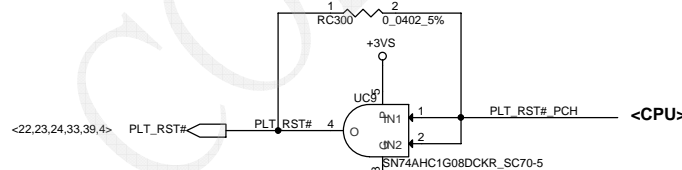
Deep S3:DSW power choose on page12

<SI>Jon : RPH15 pin swap.



<SI>Jon : Del RC117,RC118 ==>combine to RH20

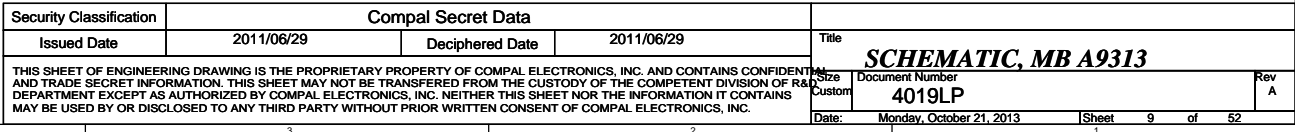
<DB>Update net name EDP\_HP\_D\_R-->EDP\_HP\_D



PD on KBC page

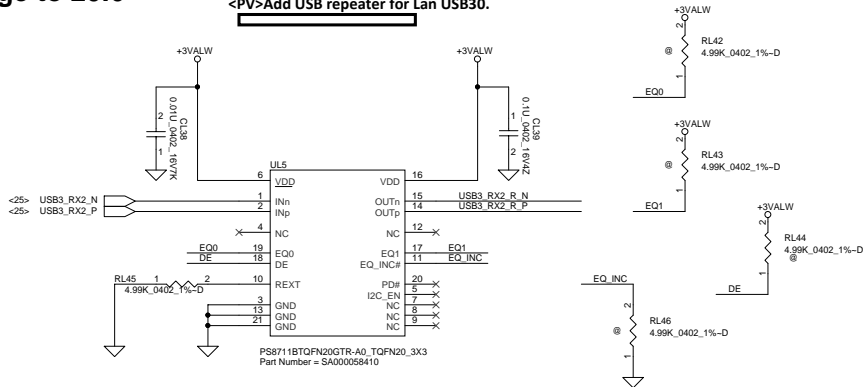
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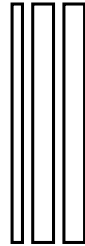
## Change to 20.6

**<PV>Add USB repeater for Lan USB30.**



Check with intel PEG which port  
Ming8/28 cancel GPU PCIE

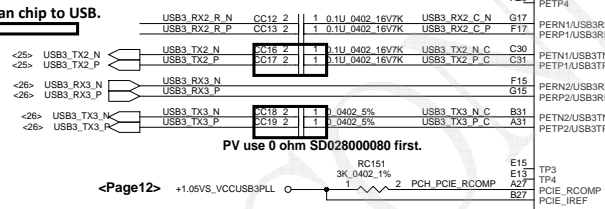
**<DB>GPU**



**<PV>Change Lan chip to USB.**

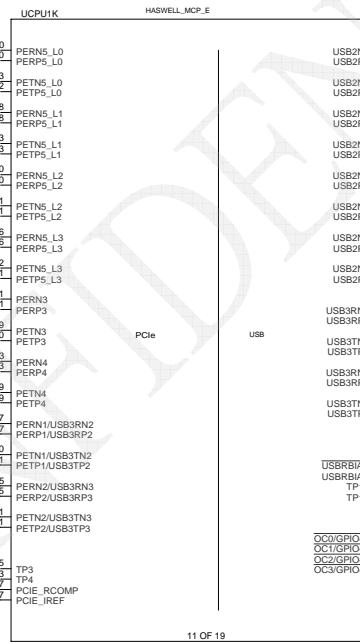
10/100/1G LAN

**<PV>Change CR chip to USB.**  
USB Card reader

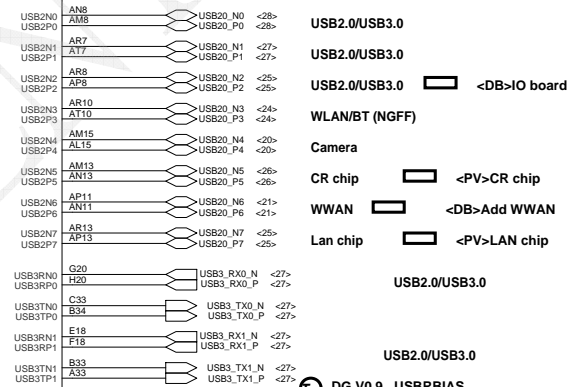


<Page12>

**Ⓣ DG V0.9 PCIE\_RCOMP**  
Width=12mil,spacing=12mil  
Max length=500mil



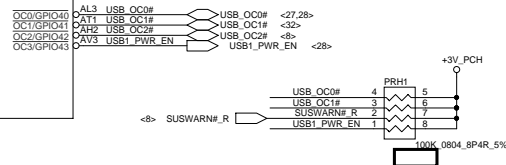
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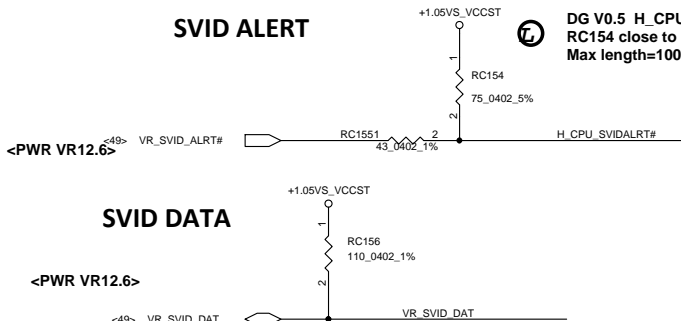
27>  DG V0.9 USBRBIAS

Trace width=50ohm and spacing=15mil  
Max length=500mil

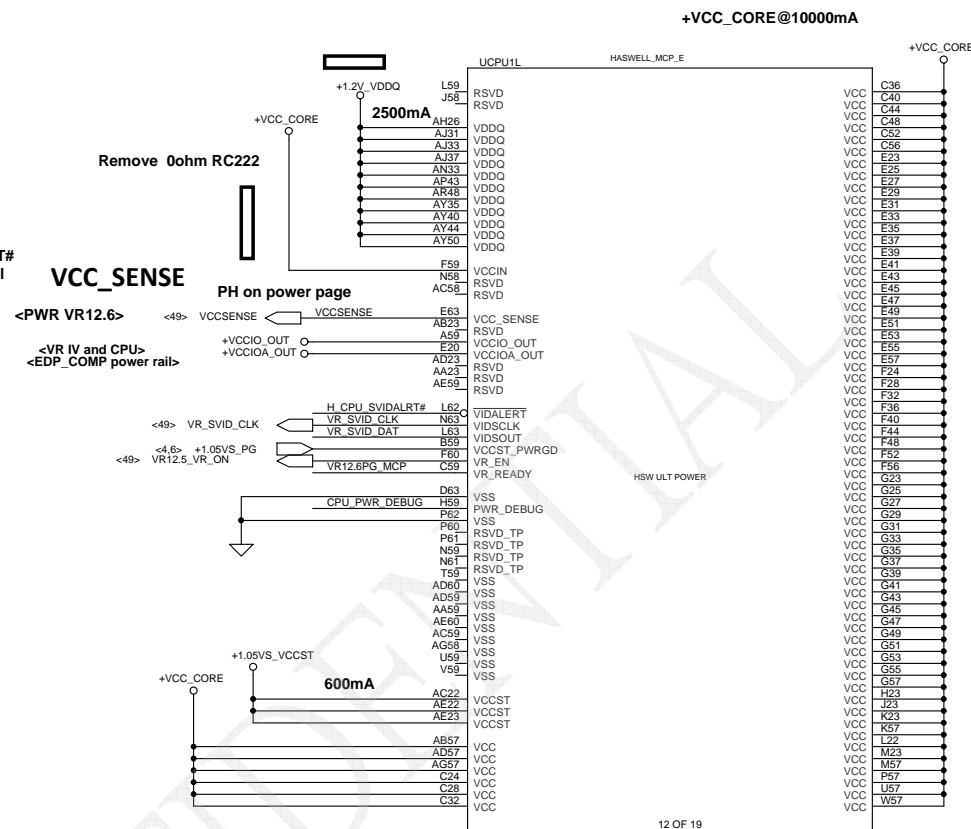
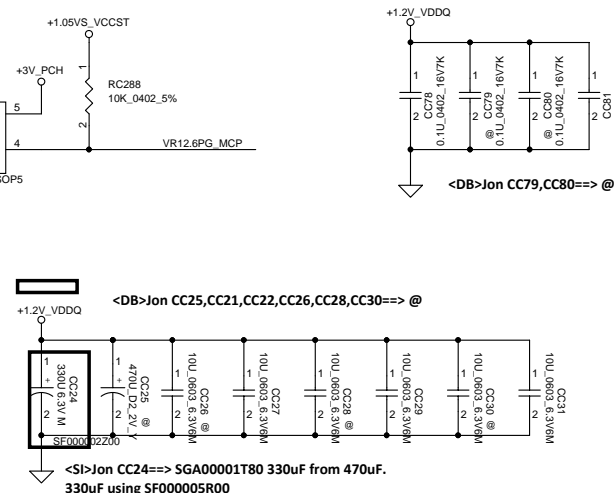
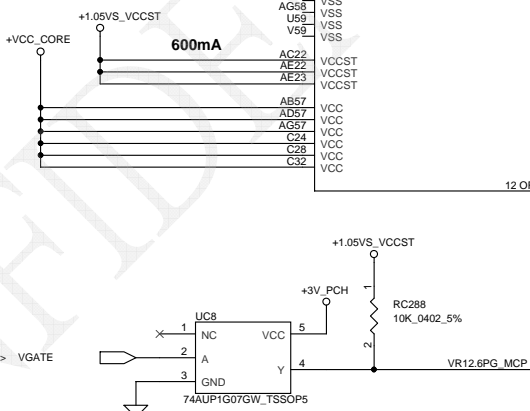
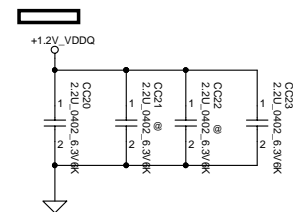
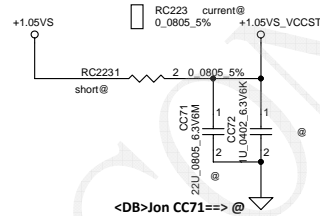
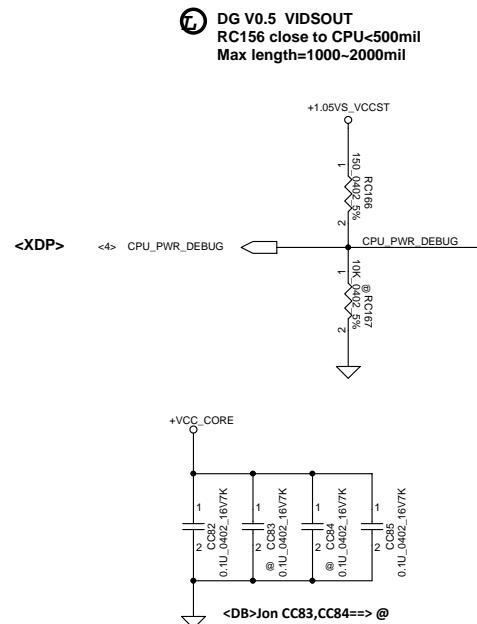
**<DB>Remove RC149 and RC150 @ part**



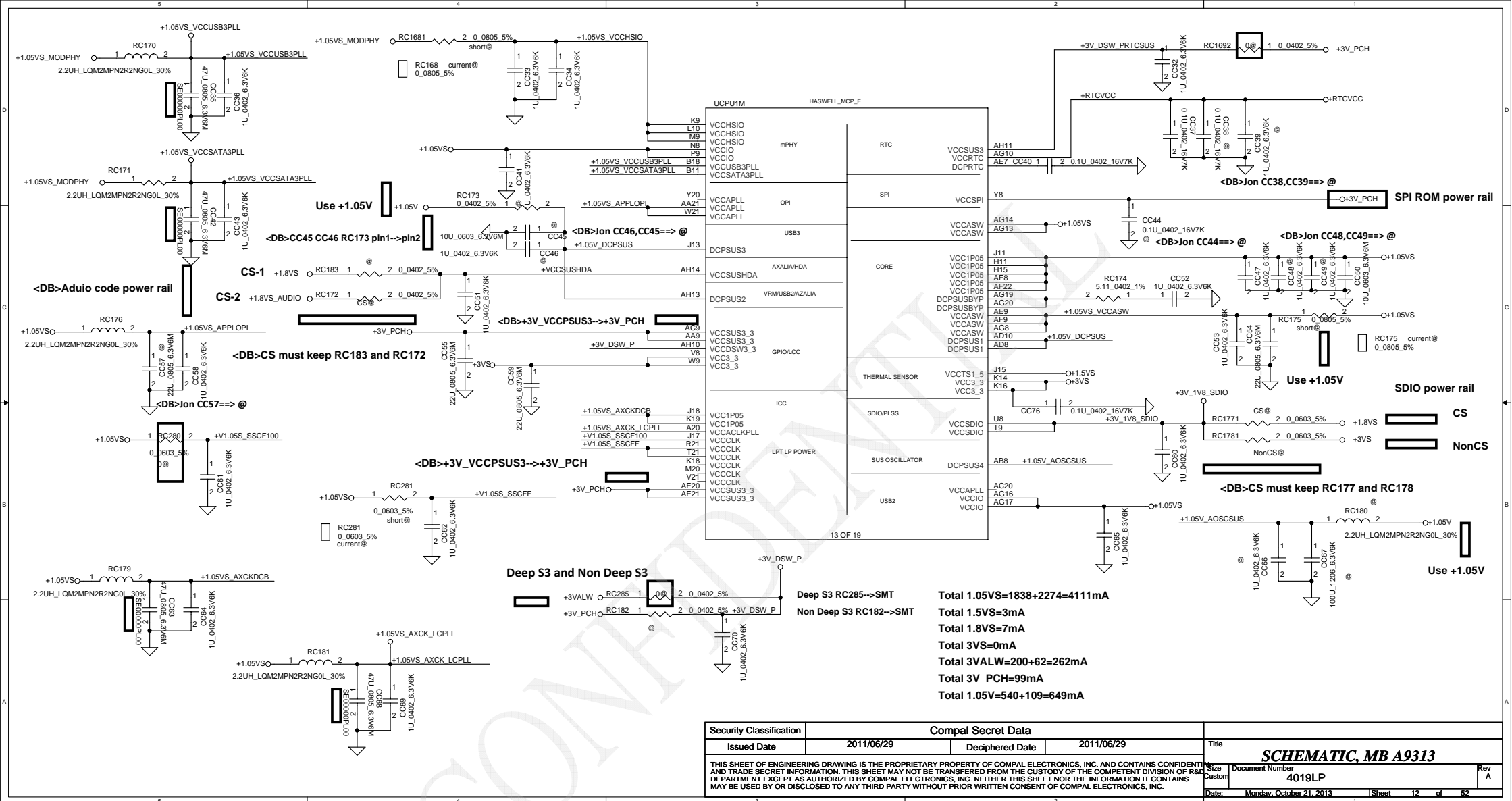
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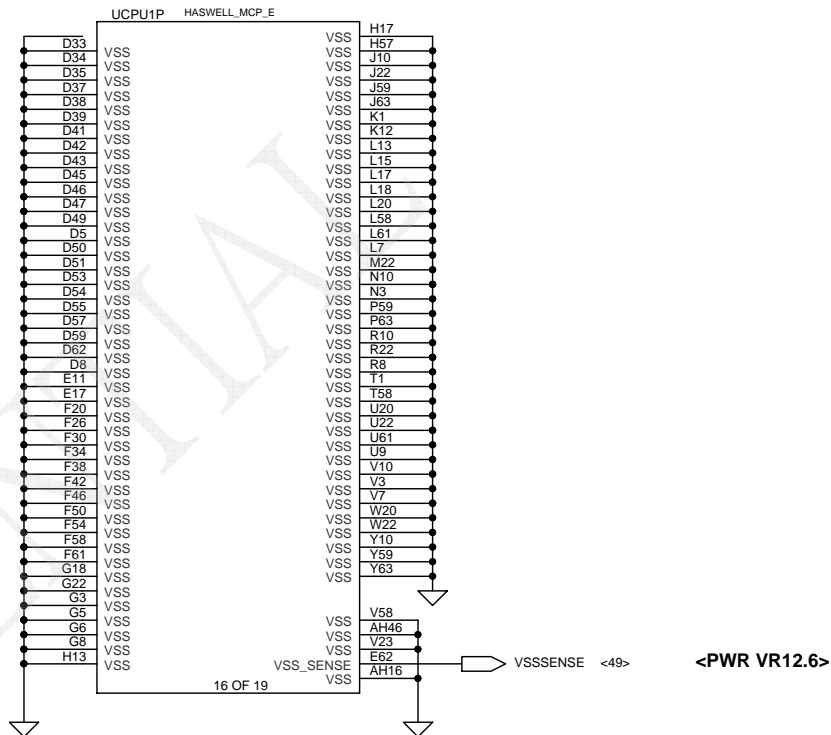
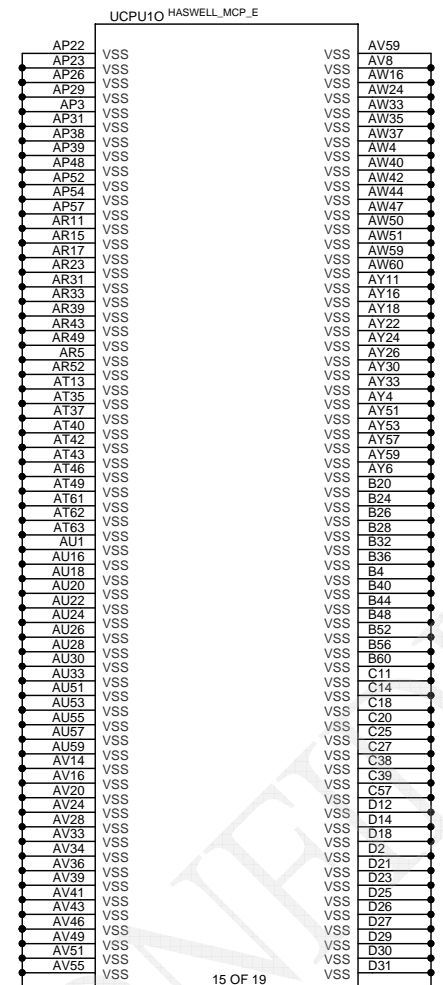
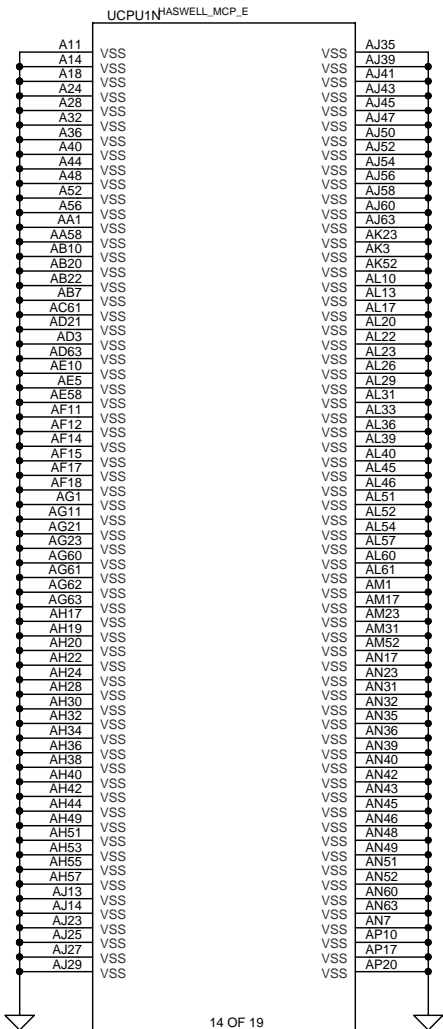


**<CPU>**

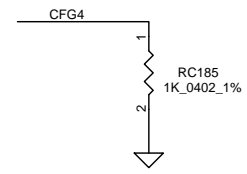
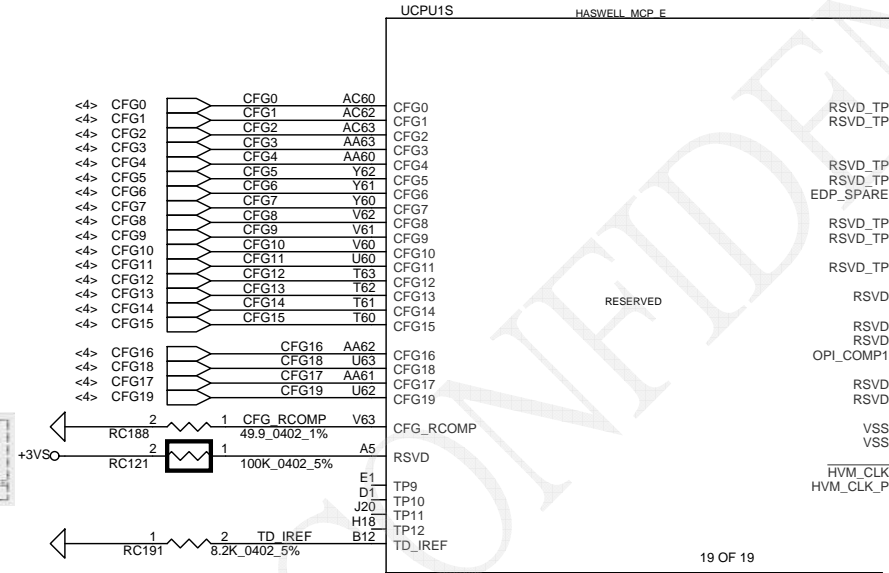
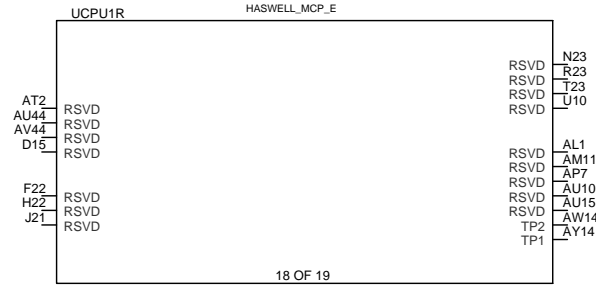
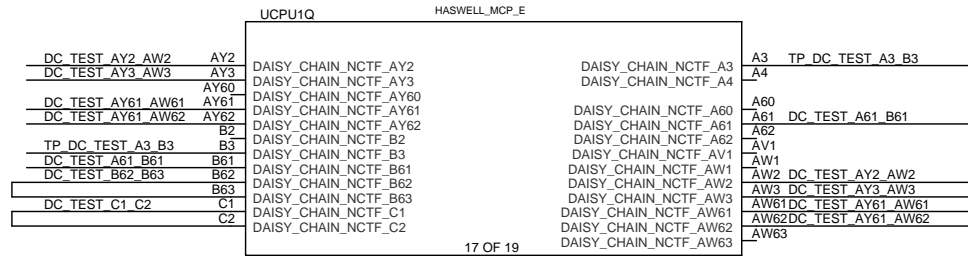


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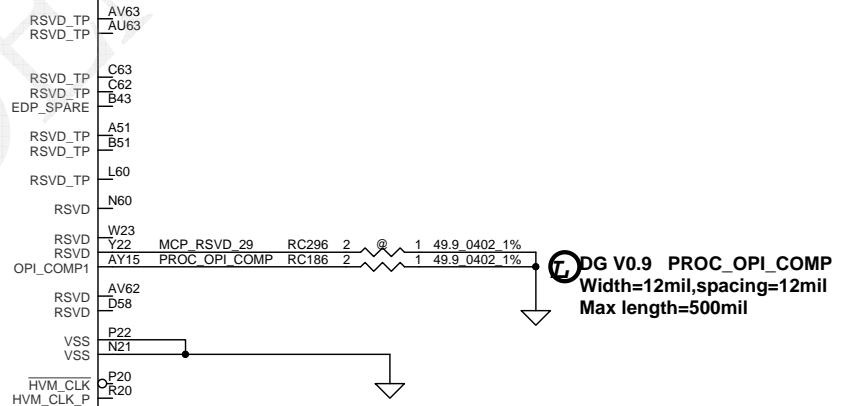
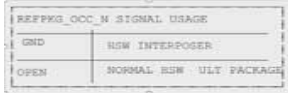


**Display Port Presence Strap**

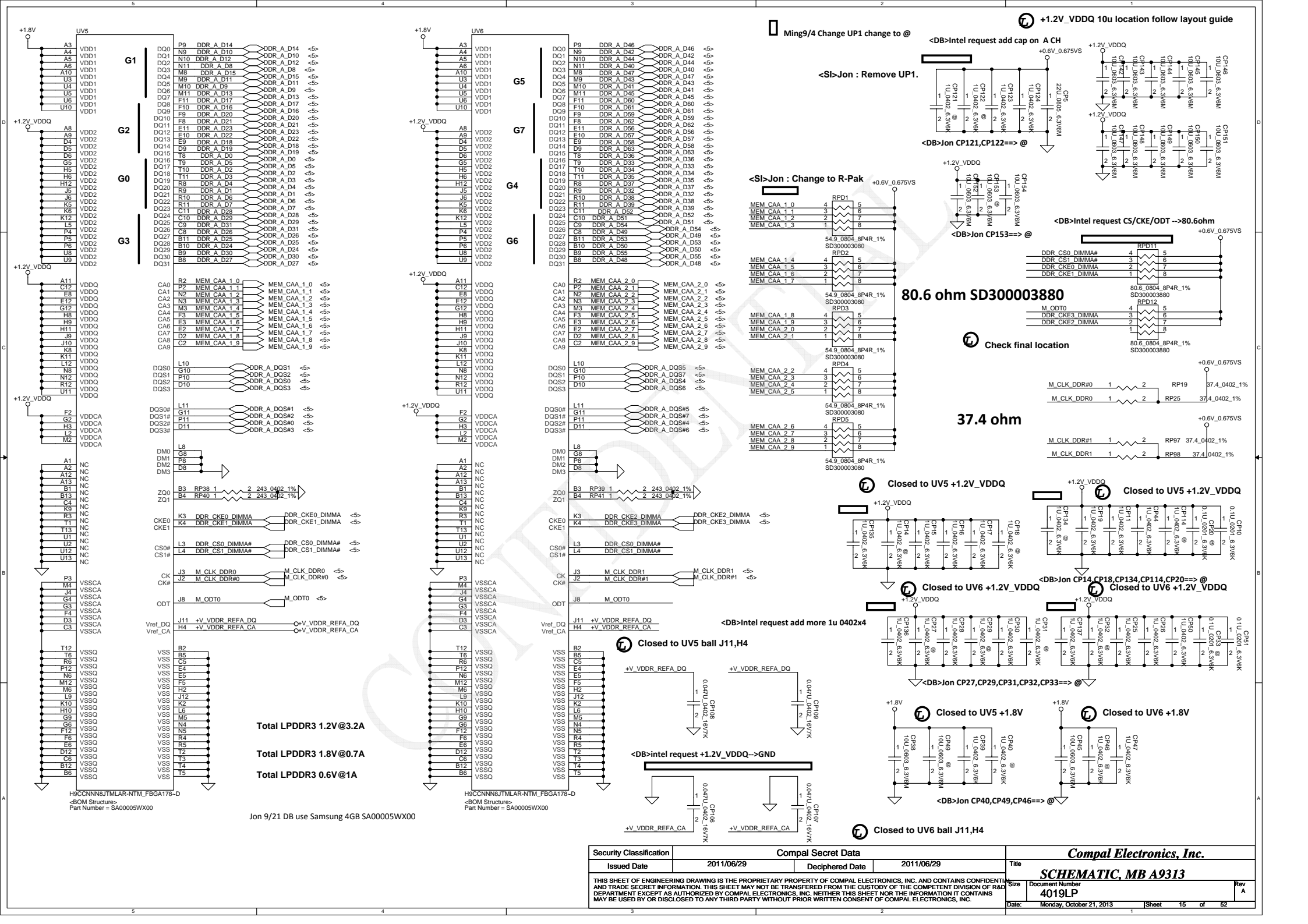
**CFG4**

**1 : Disabled; No Physical Display Port attached to Embedded Display Port**

**\* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port**



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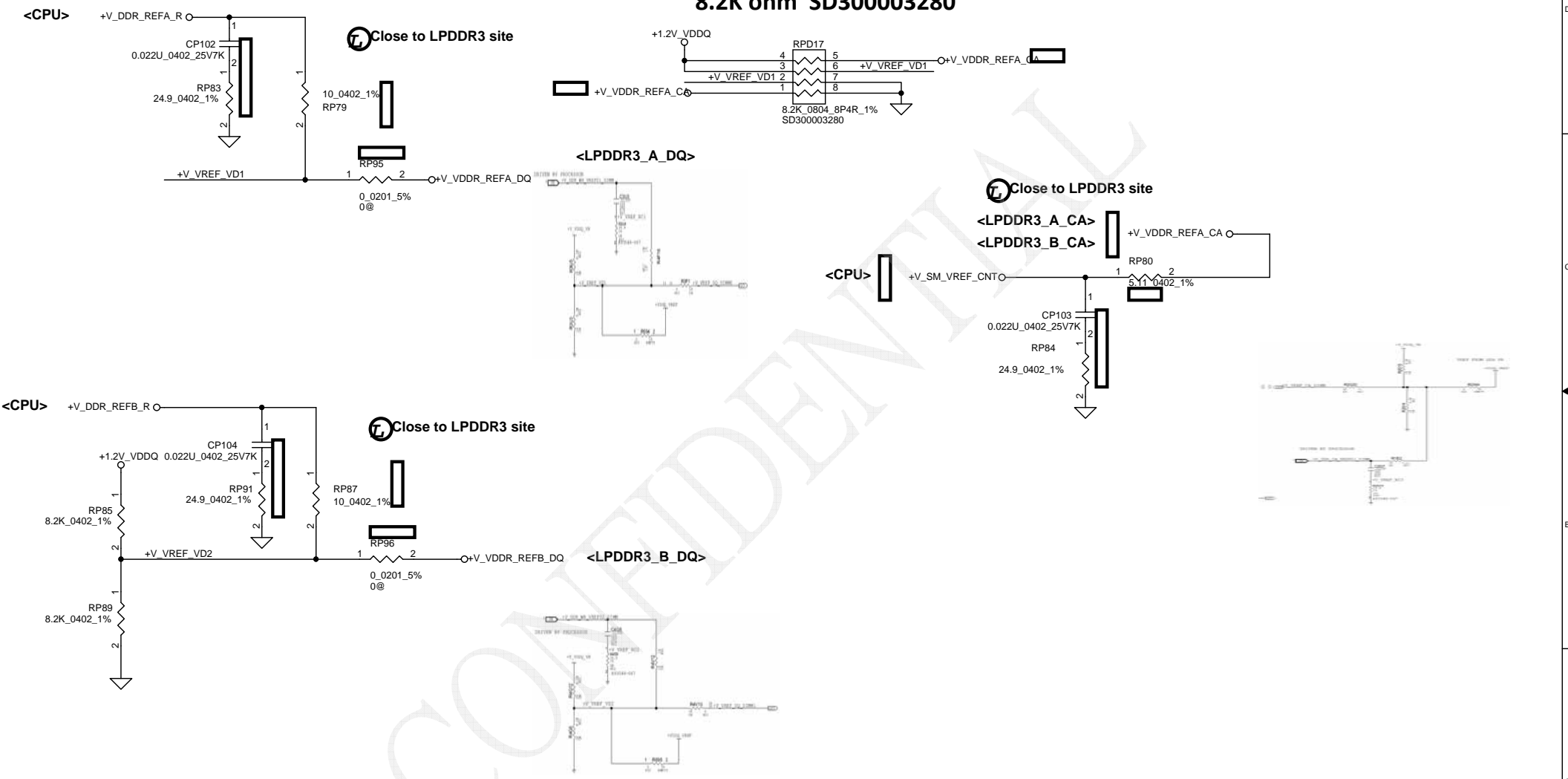




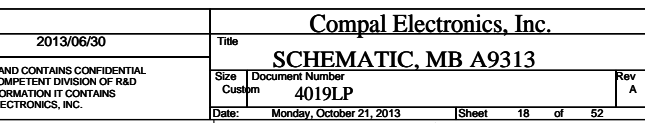
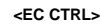
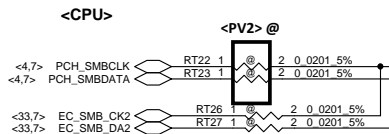
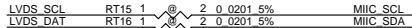
LPDDR3 VREF

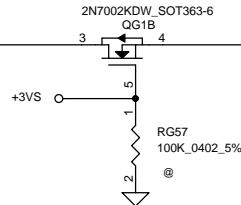
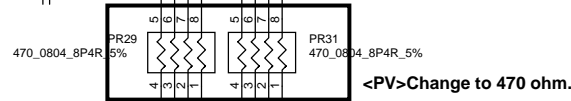
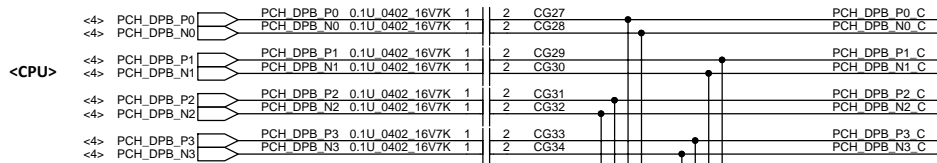
<PV>Modify Vref circuit.

8.2K ohm SD300003280

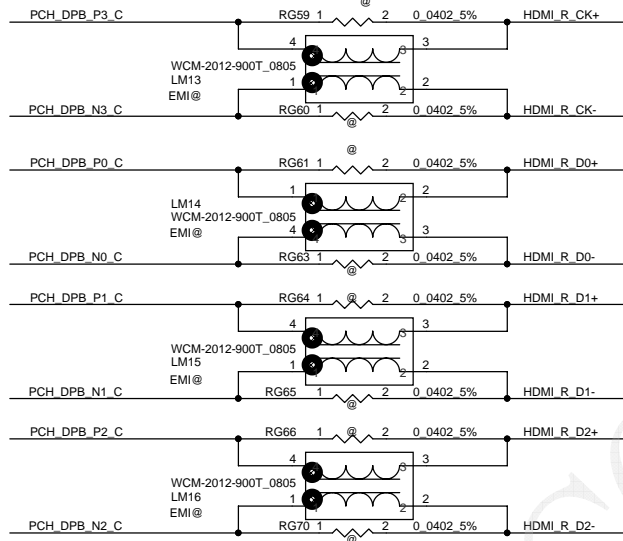


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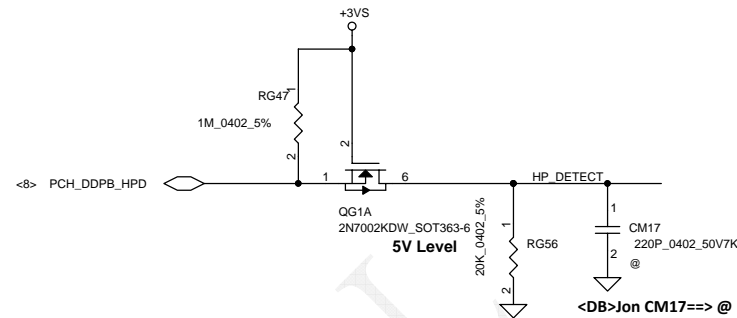
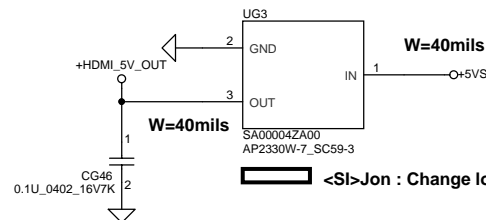
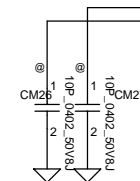
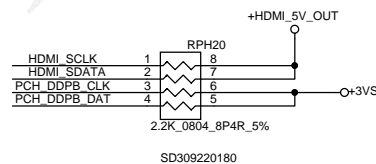


## EMI@ Change to 47.1



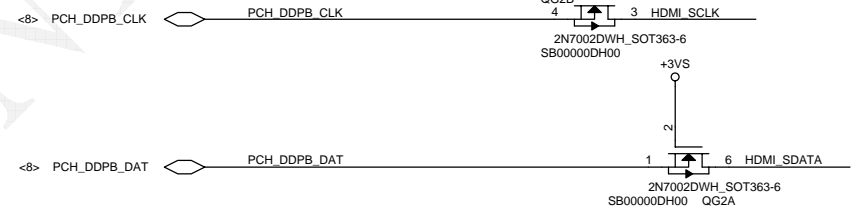
<Sl>Jon : Del CM18~CM25.

<Sl>Jon : Change to R-PAK.



Ming9/11 remove RG58/RG62 for double PU to CPU side

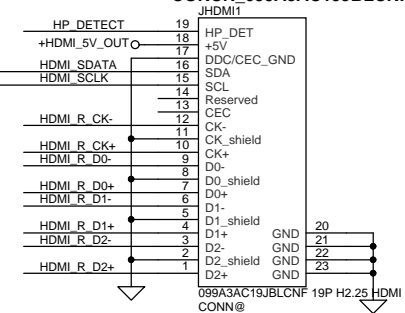
Follow Intel  
Feedback putting  
2.2K ohm



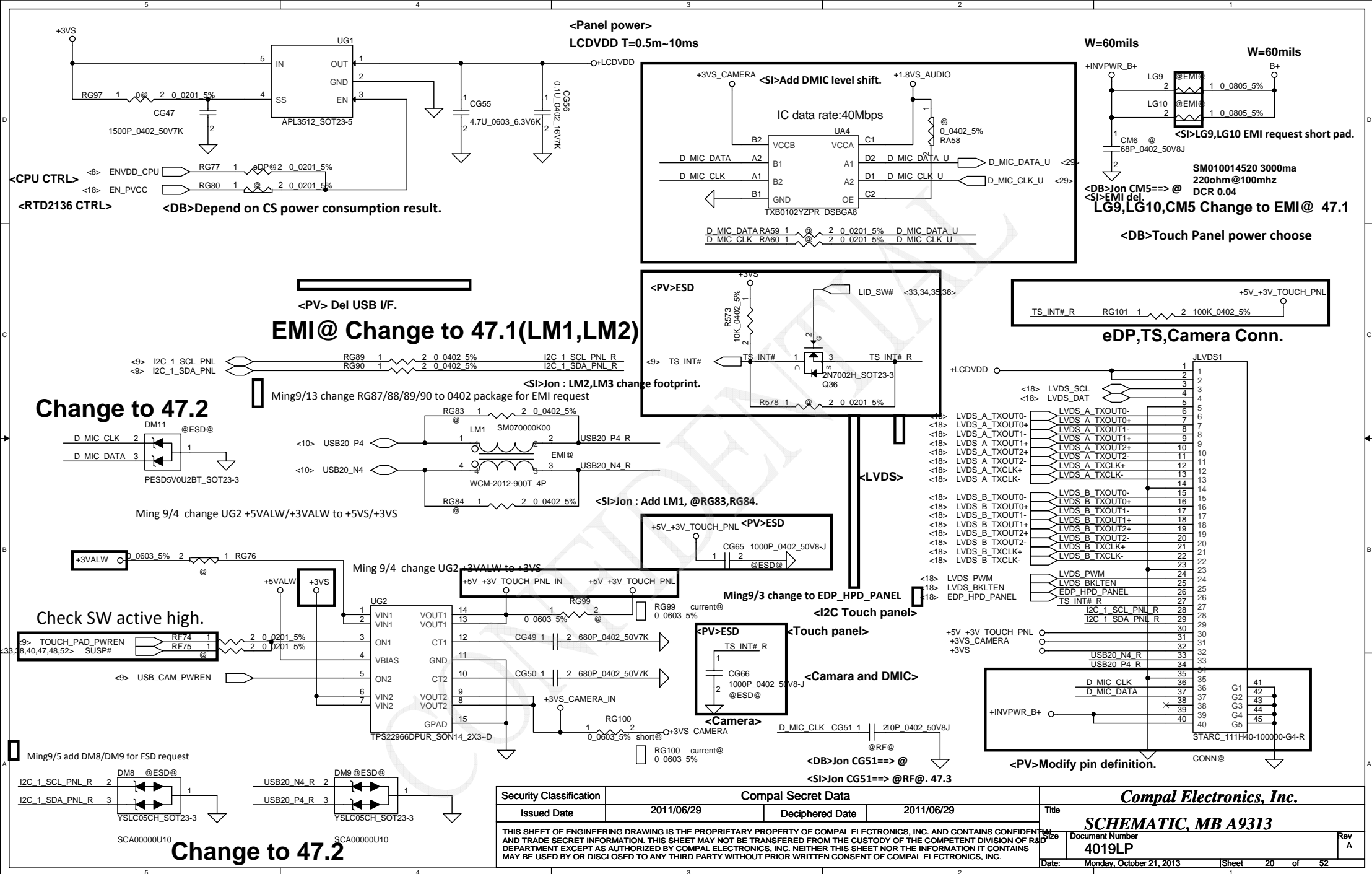
5V PULL UP IN CONNECTER SIDE

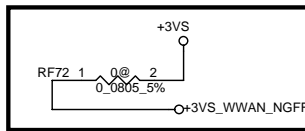
## HDMI Conn.

<Sl>Jon : Change footprint to  
CONCR\_099A3AC19JBLCNF\_19P-T



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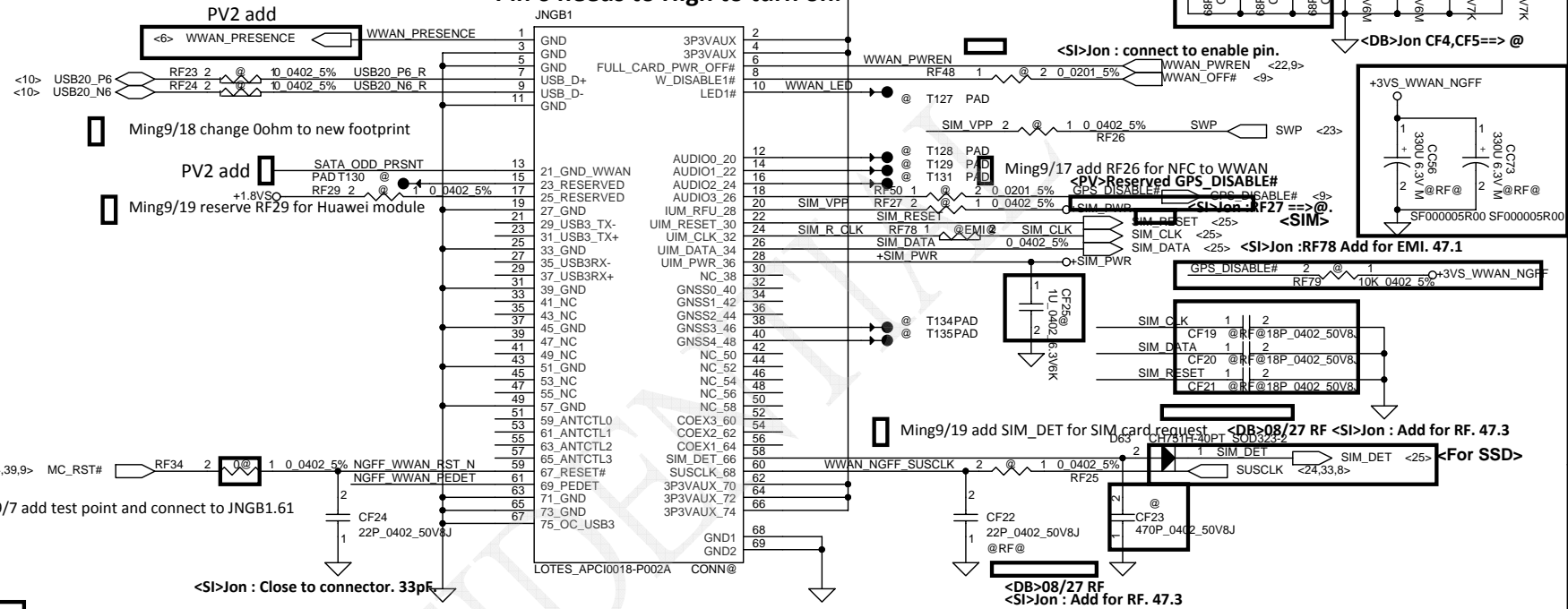




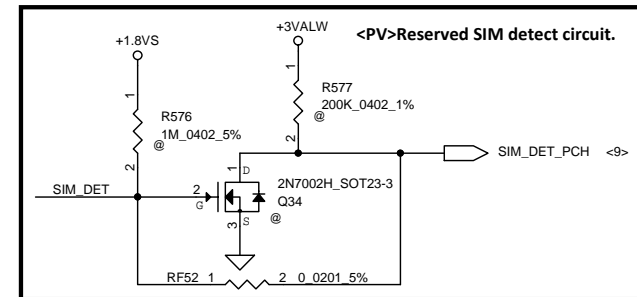
Check connector footprint  
8/27 update footprint

## WWAN NGFF\_B

Pin 6 needs to High to turn on.

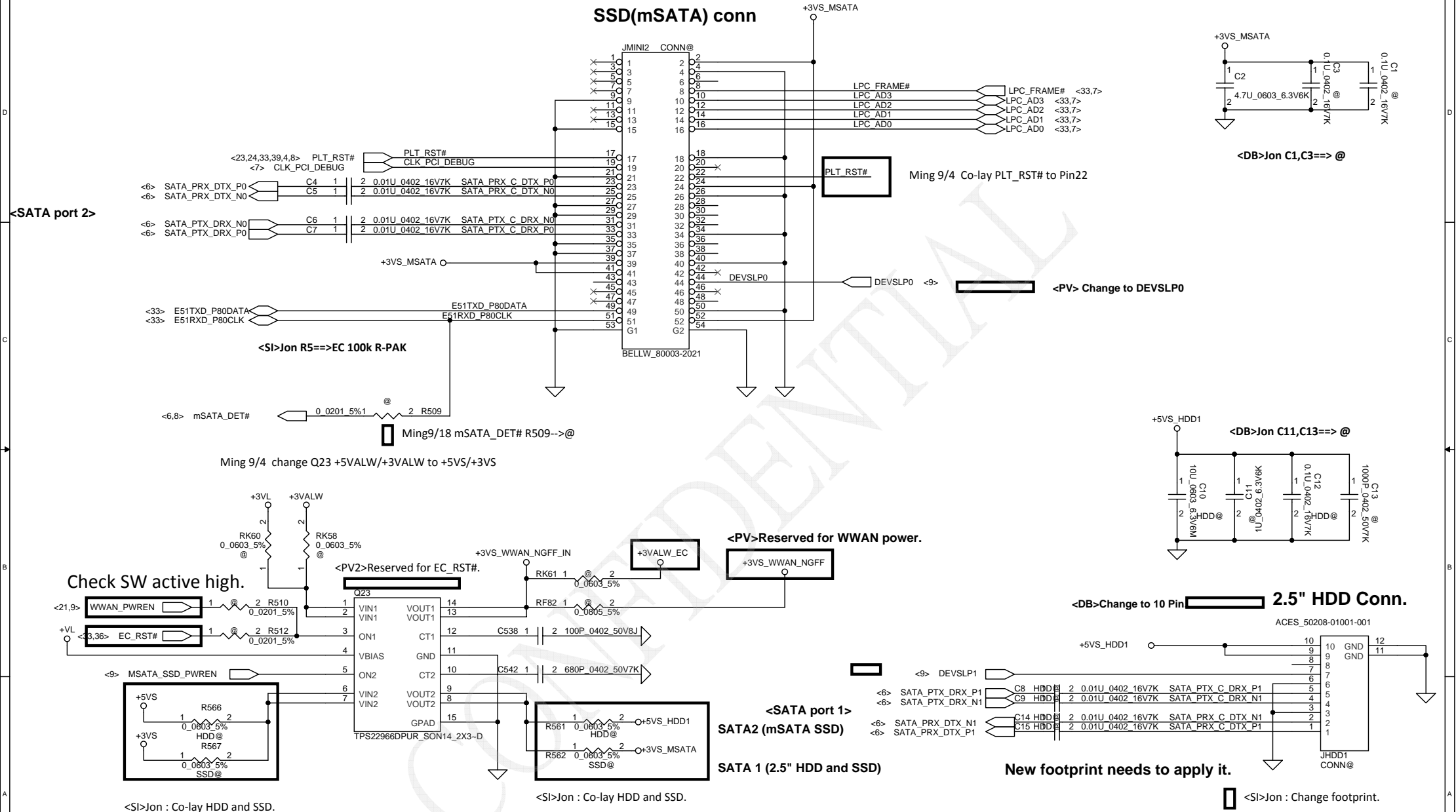


# Check circuit connection.

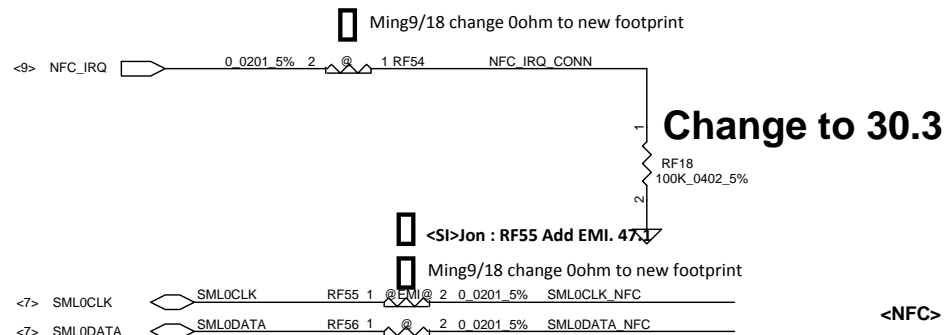


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# SSD(mSATA) conn



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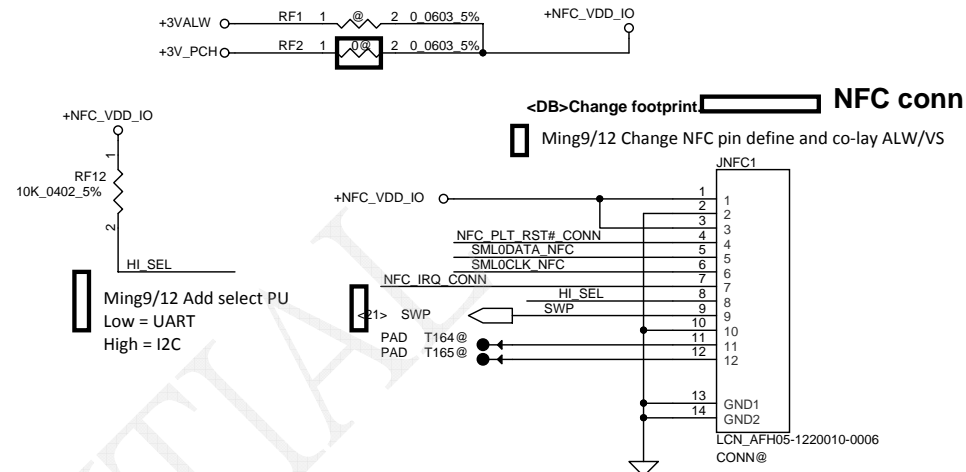
Ming9/12 remove NGFF connect

Ming9/12 ref#498872  
FOR NXP SUPPORT (DEFAULT)

Ming9/12 add UF1/UF2 for intel check list



<SI>Jon : Change footprint to 74AHCT1G08GV\_SOT753-5



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+3VS\_WLAN\_NGFF

## WLAN NGFF\_E

<DB>Intel request Signal swap (USB N and P)

SDIO

PCI-E WLAN(NGFF).Default:SDIO

Ming9/19 change PCIe pin define for NGFF connector

<DB>Update net name

<DB>Add PH on SDIO\_0\_DATA0~DATA3,CMD

<SI>Jon Power rail to +3V\_1V8\_SDIO

SDIO@

Ming9/13 change SDIO\_D[3:1] 20 K to 47K for Intel request SDIO\_CLK/SDIO\_CMD to 150K

<SI>Jon : for WLAN sequence.

Ming9/18 change UF4 to dual MOS

Ming9/7 add RF50 for PLT\_RST# debug

Level shift intel use Fairchild FXM21C102

Choose TI solution TXS0102YZPR

Ming9/19 add RF42, CF23 for reset circuit for Intel request

Del RL34,RL36

Change to 30.3

+3VS\_WLAN\_NGFF

+3VS\_WLAN\_NGFF

Ming9/7 add MINI1\_LED# for ID

<WLAN\_NGFF>

<DB>Intel request Signal swap (RX and TX)

<SI>Jon :Request by Dean.

<WLAN\_NGFF>

Ming9/12 remove NGFF connect with NFC

Ming9/18 change 0ohm to new footprint

<WLAN\_NGFF>

<WLAN\_NGFF>

WLAN\_NGFF

CF18 ==>Change to 32.3

WWAN\_NGFF

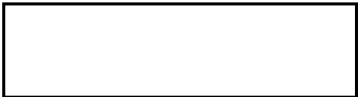
Ming9/13 reserve RF72/73/74/75 for Intel request

<SI>Jon UART PH to connector side.

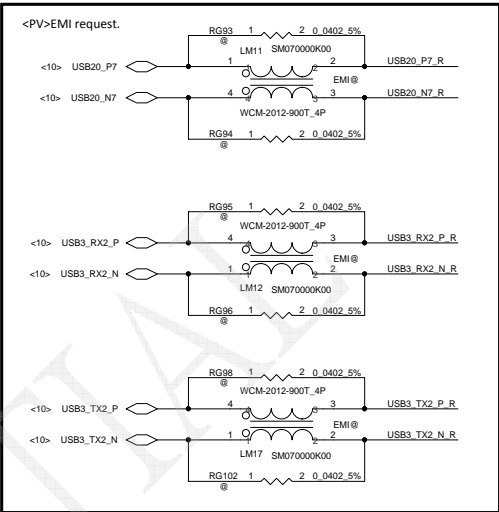
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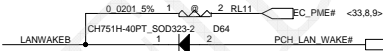
Change to 20.6



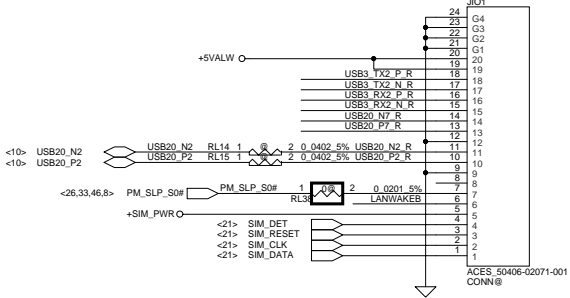
<PV>Change Lan IC to USB in subboard.



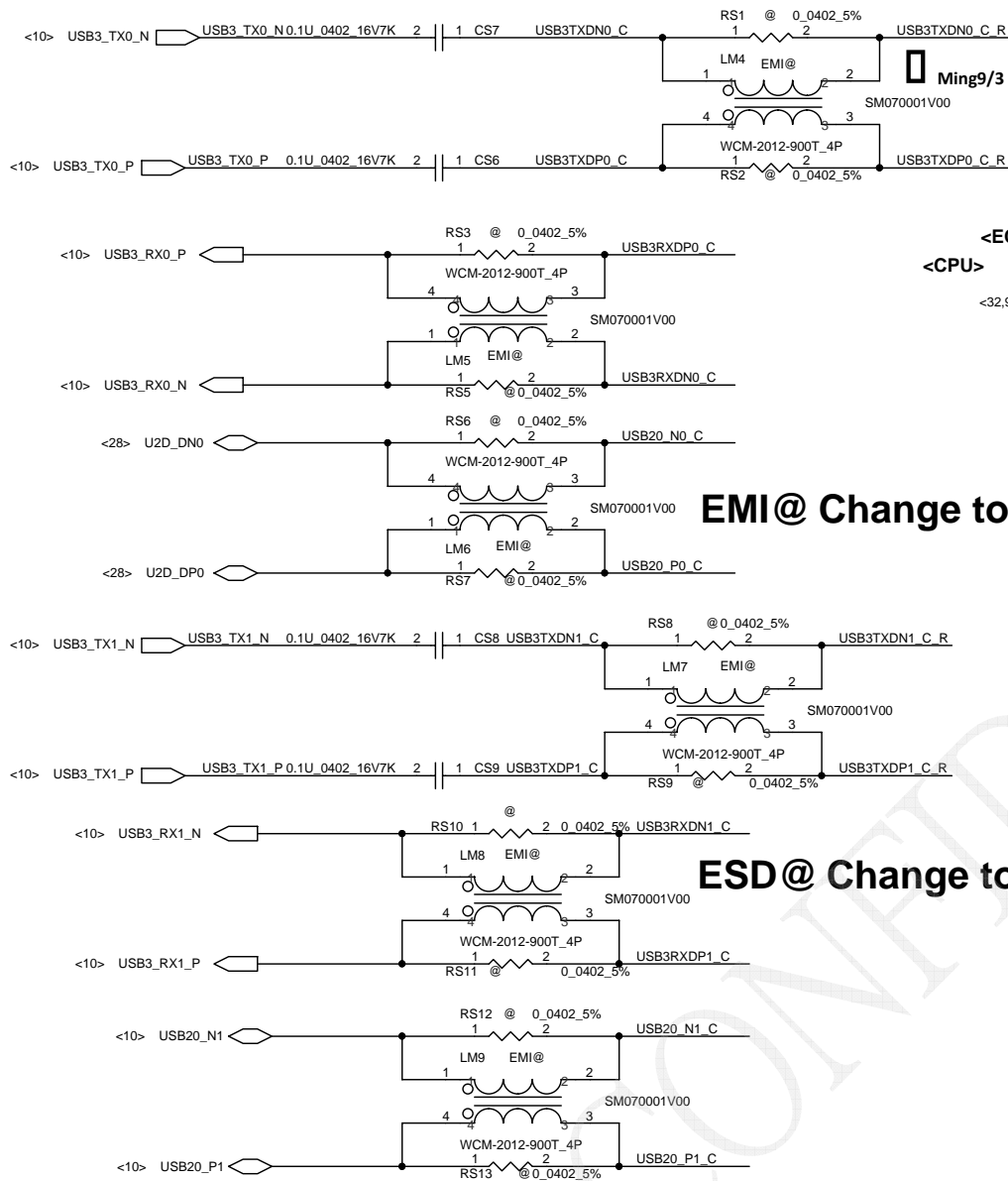
<PV>Change connector pin definition.  
<PV>Swap pin definition.



<PV>RL12 change to D64 for power leakage.







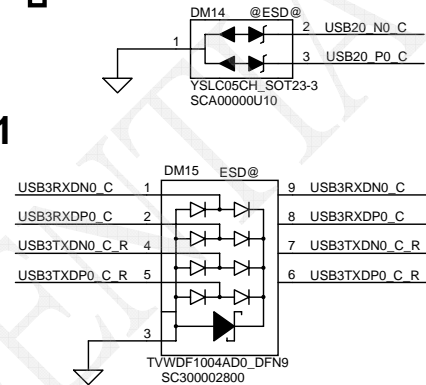
**EMI@ Change to 47.1**

**ESD@ Change to 47.1**

**<EC>  
<CPU>**

**CS10~CS13,US2 Change to 7.6**

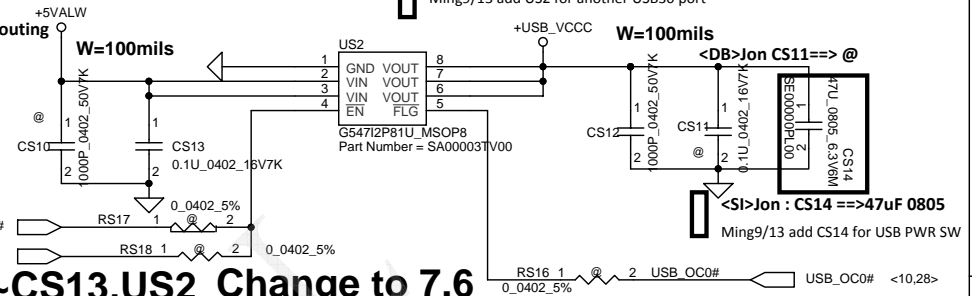
Ming9/5 Change DM14/DM15/DM16/DM17 symbol for ESD request



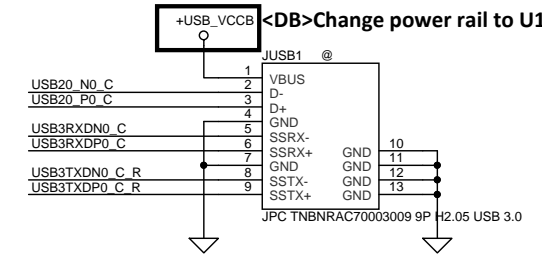
**ESD@ Change to 47.2**

**USB3.0 need support 2.5A  
change USB PWR SW SA00003TV00  
low active**

Ming9/13 add US2 for another USB30 port

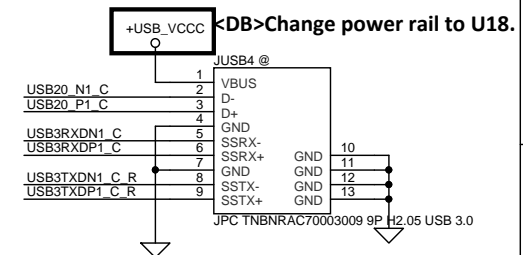


**<DB>Update footprint to DC233008M10.  
USB2.0/USB3.0 port 1**

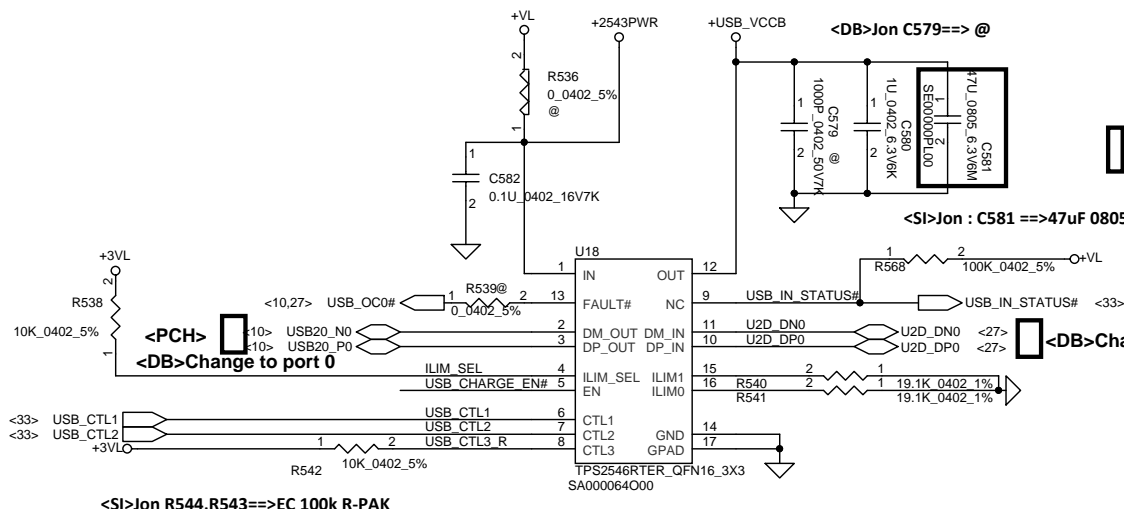


**<SI>Jon : Change footprint to  
J-L\_TNBNRAC70003009\_9P-T**

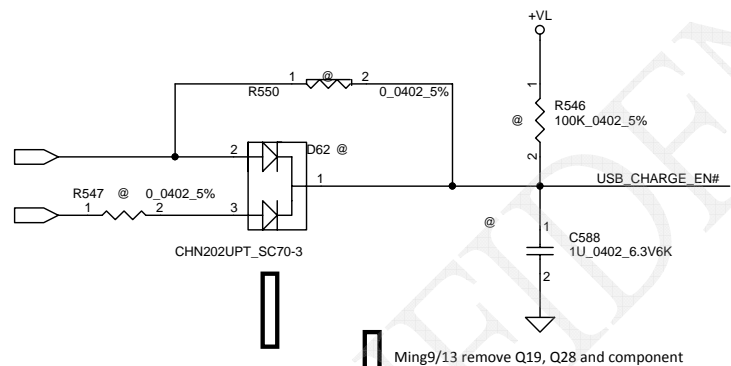
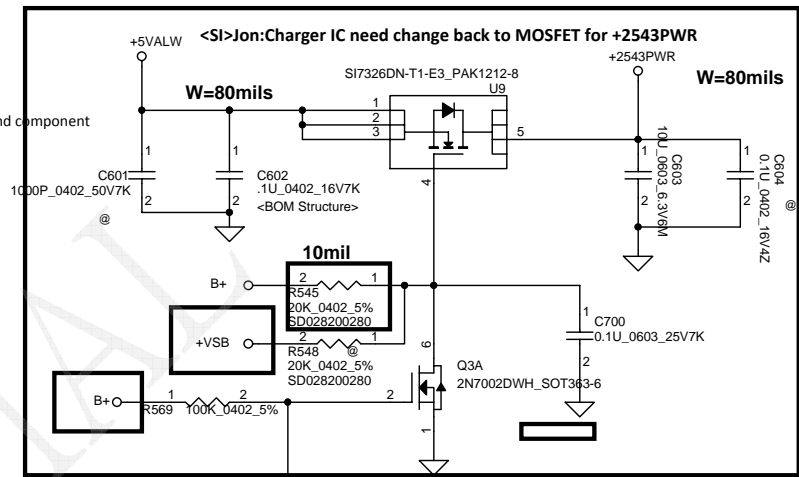
**USB2.0/USB3.0 port 2**



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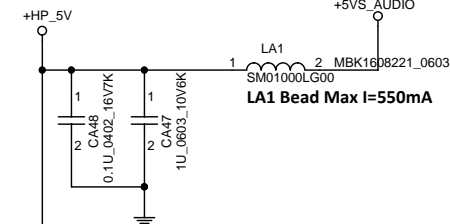
Ming9/13 remove Q26 and component



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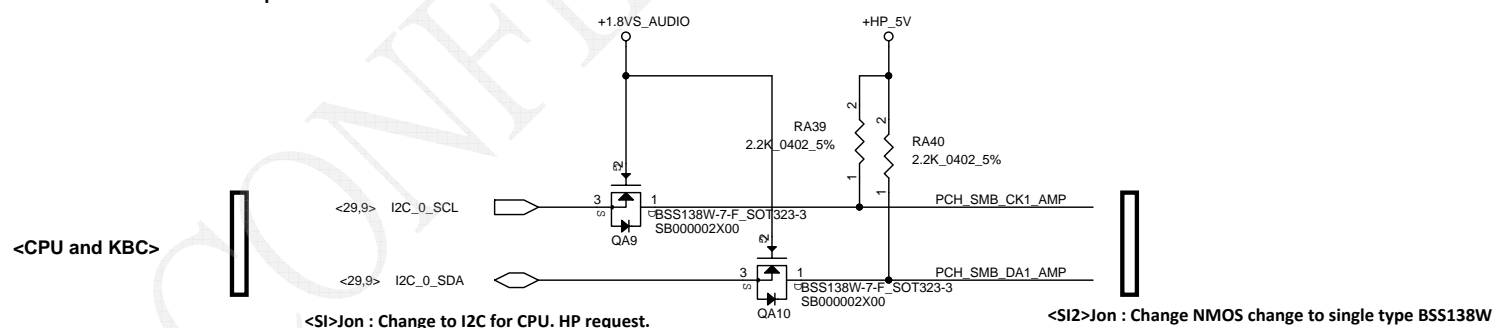




LA1 Bead Max I=550mA

<SI>Jon : RA26,RA29 Change to 30 ohm 1%.

<DB>2012-09-06 : Move beed to sub board



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Cap and R closed to JIO1 conn

Ext. Mic

<DB>2012-09-10 :

Mono Mic : use 2.2kohm  
Stereo Mic : use two 4.7ohm  
in parallel for 2.2kohm

<CONN and Codec>

PCH\_HP\_DET  
High : Enable (HP Plugin)  
Low : Disable (No HP)

<to Codec>

<DB> Codec Internal  
Pull up to PVDD  
<from CONN>

The jack is norem open

<DB> 2012-09-10 : Change the  
HP\_DET Logic for Codec

<SI>Jon : change to dual 2N7002.

<DB> Follow IDT Reference Circuit

Pull High on CPU site

PCH\_MIC\_DET#  
High : Disable (No MIC)  
Low : Enable (MIC Plugin)

<SI>Jon : change to dual 2N7002.

SPK conn

<SI>Jon :CA70,CA69 Add for EMI.47.2

JSPK1

Ming9/10 Change Connector symbol

USB3.0 need support 2.5A  
change USB PWR SW SA00003TV00  
low active

Change to 7.6

<PV>Del LANC\_B\_DET#\_PCH.

	PCH_HP_DET (GPIO53)	PCH_MIC_DET# (GPIO51)
Internal MIC	Low	X
External MIC (headset)	High	Low
Internal MIC (Headphone)	High	High

<DB>  
2012-09-06 : Change Pin Define and Add AGND to 3pins  
2012-09-10 : Change AGND from pin12 to pin14.  
SPKR+/SPKR- change to pin12/pin13.  
Because class-D speaker trace should refer to DGND NOT AGND.

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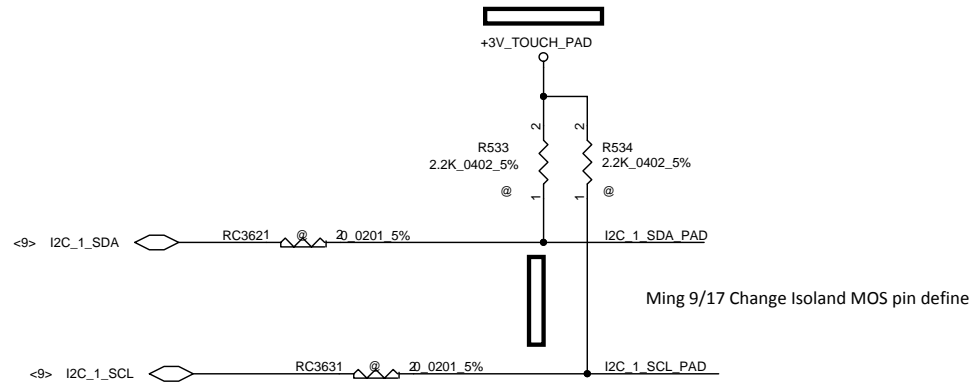




## Keyboard conn

&lt;SI&gt;Jon : Del power switch mos.

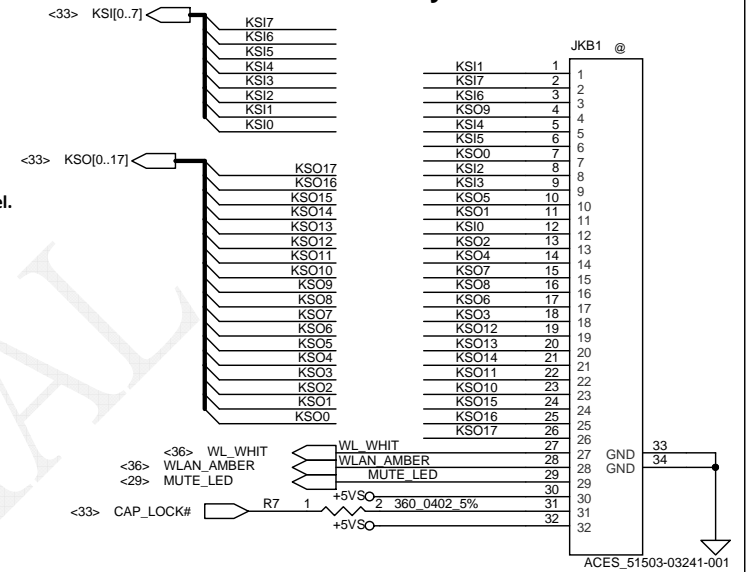
&lt;DB&gt;Jon C539==&gt; @



&lt;SI&gt;EMI request : Del.

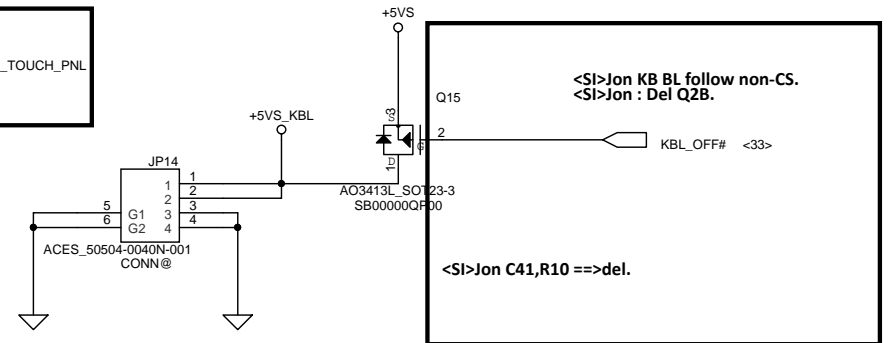
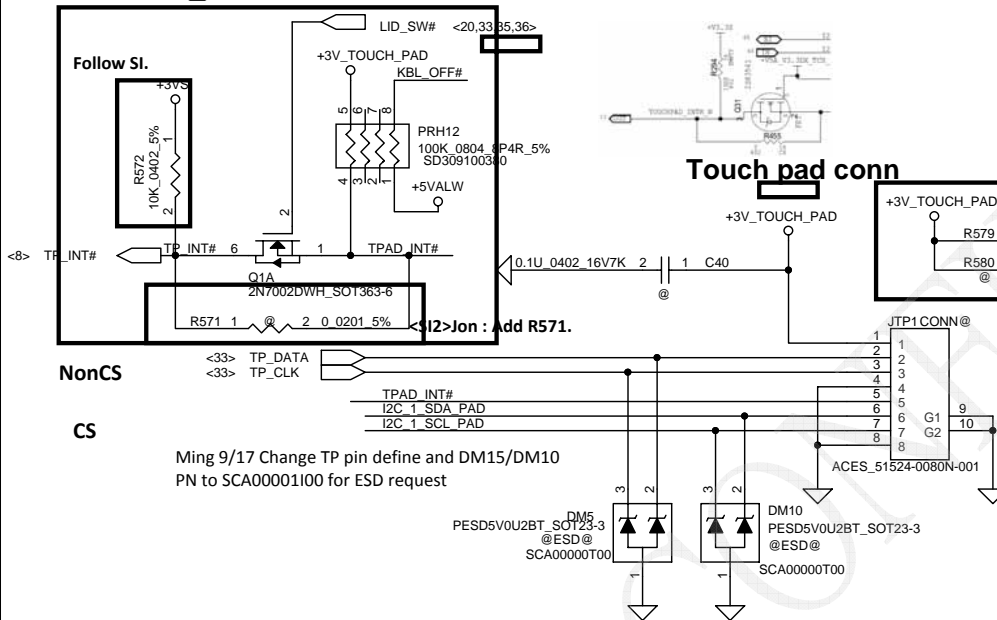
&lt;DB&gt;Jon all Cap==&gt; @

&lt;SI&gt;Jon all Cap==&gt; @EMI@. 47.1



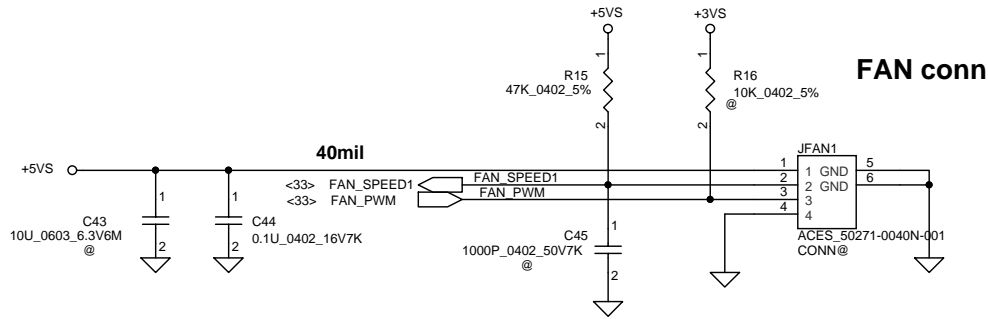
&lt;SI&gt;Jon KB pin1 ==&gt;KSI1

## Keyboard backlight Conn

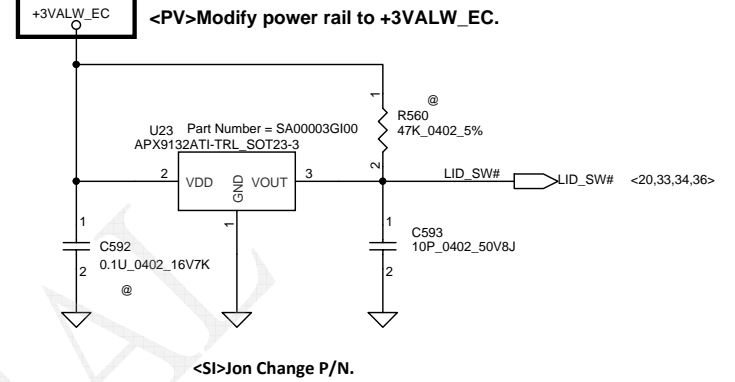


&lt;SI&gt;Jon C41,R10 ==&gt;del.

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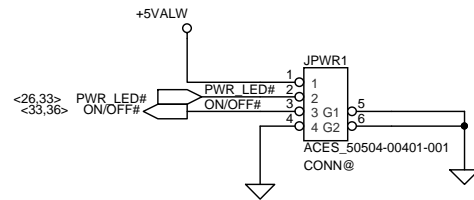


## Lid Switch (Hall Effect Sensor)



<DB>Change to subboard.

Ming9/12 change to PWR/B

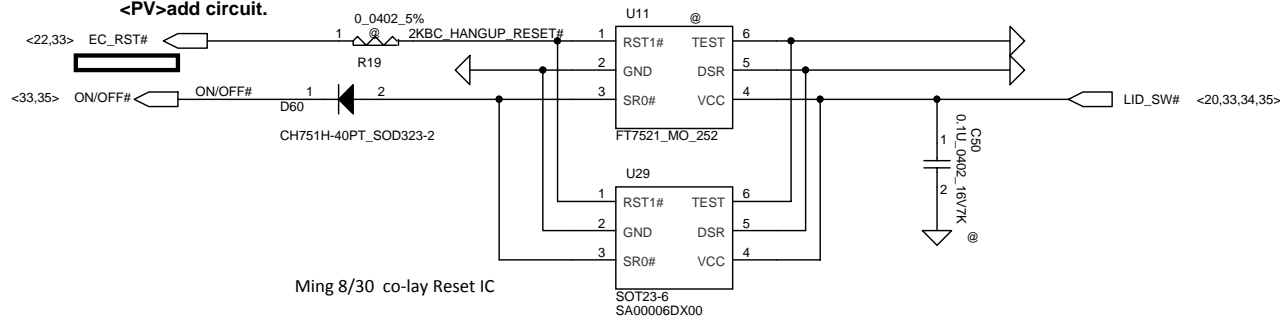


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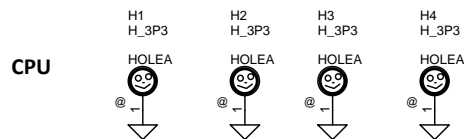
# Reset IC

No ENTRIP1 and ENTRIP2 on page , need to study

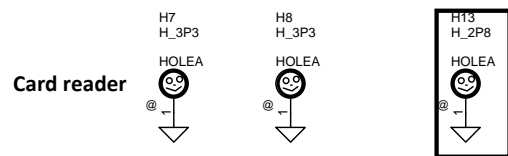
<PV>add circuit.



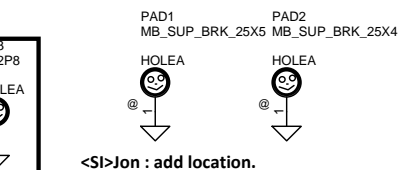
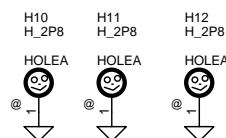
Ming 8/30 co-lay Reset IC



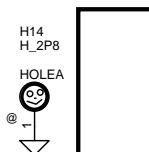
GPU



Card reader



<SI>Jon : add location.

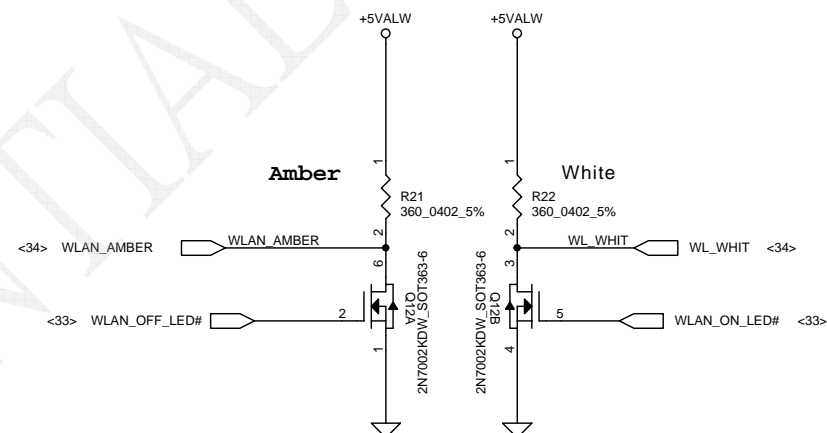
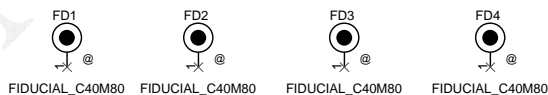


<SI2>Jon : Del H15.



PCB

ZZZ1  
LA-9313P  
DAA00065000

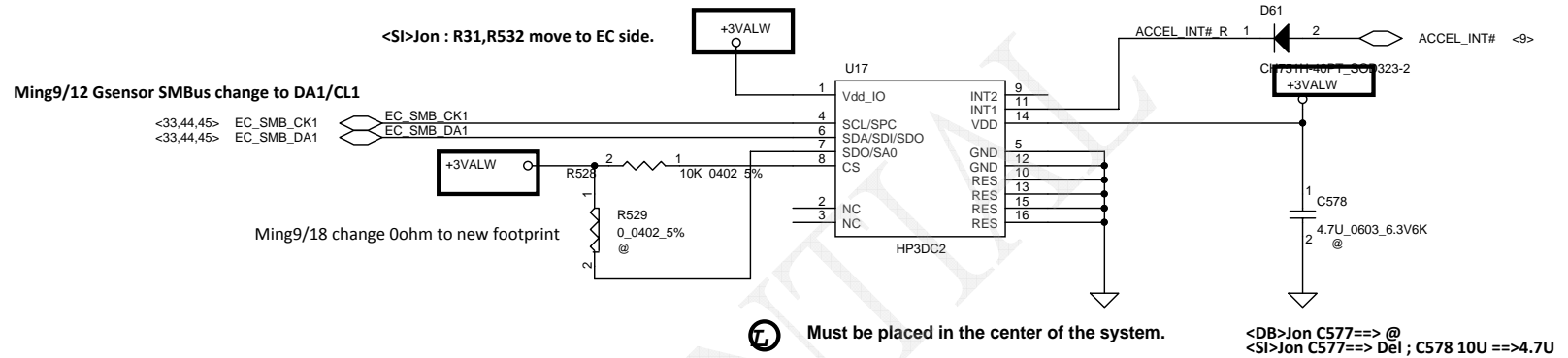


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# ACCELEROMETER

Ming8/29 Gsensor change to +3VALW

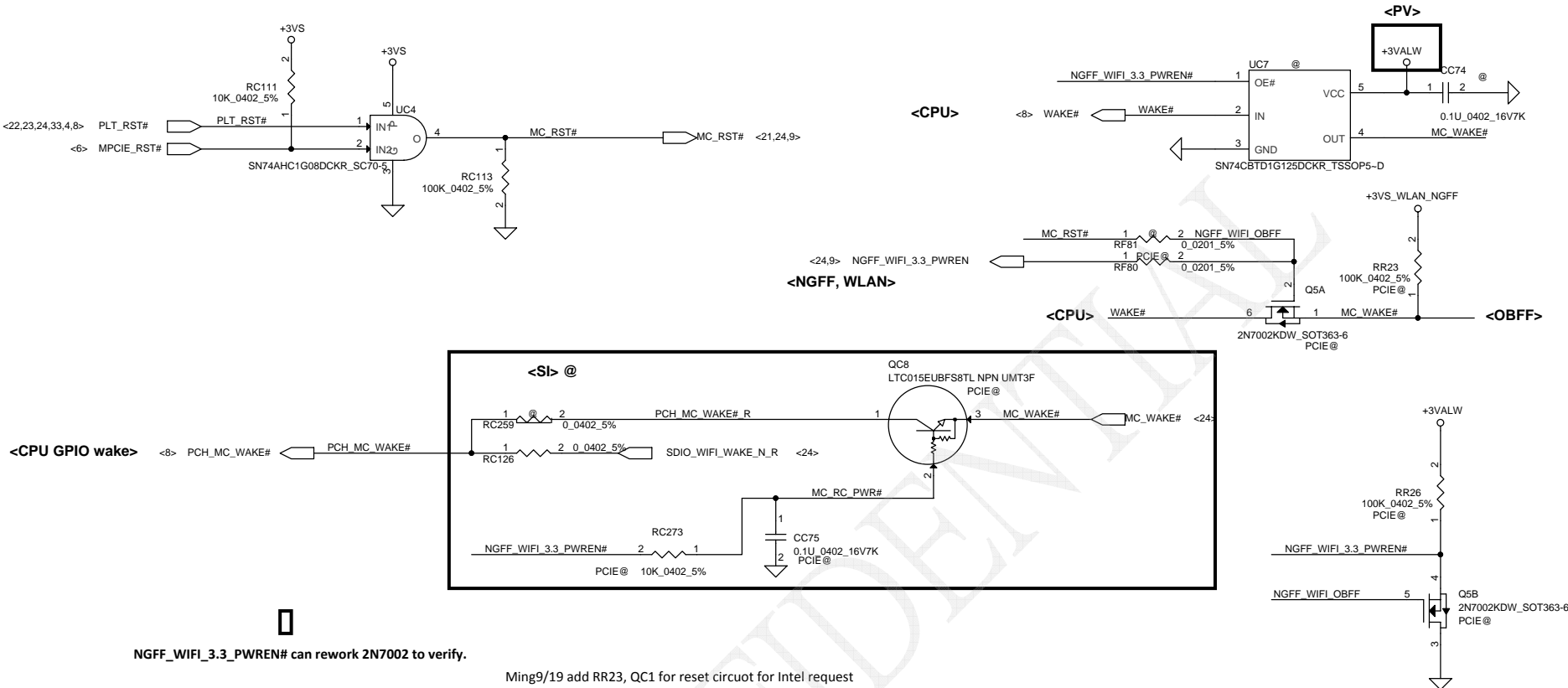
Sensor hub -->G-sensor



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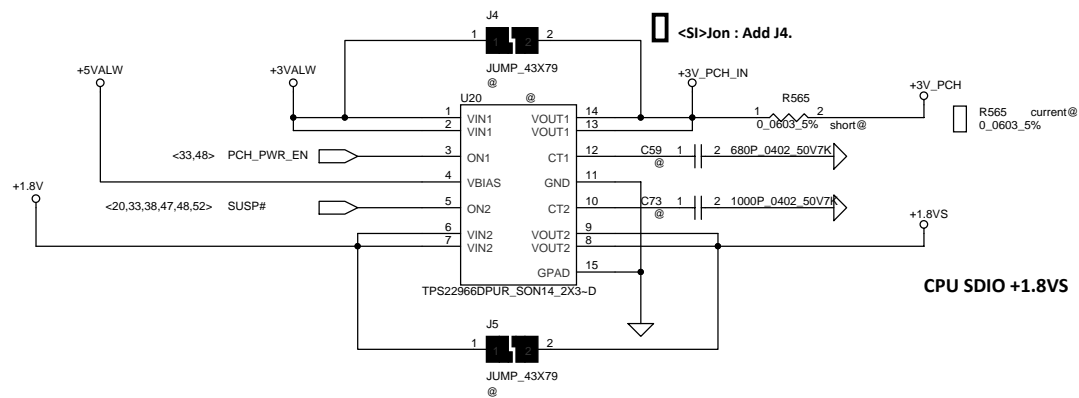
NGFF and WLAN



NGFF\_WIFI\_3.3\_PWREN# can rework 2N7002 to verify.

Ming9/19 add RR23, QC1 for reset circuit for Intel request

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Verify +3V\_PCH to ALWS

1. S4/S5 shutdown ALWS power (under no WOL)

2. S4/S5 turn on ALWS power (under WOL)

Verify +1.8VS to +1.8V

1. PCH's VCCSUSDA change to +1.8VS\_AUDIO to verify CODEC RTD3 cold feature.

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Headphone and Mic conn

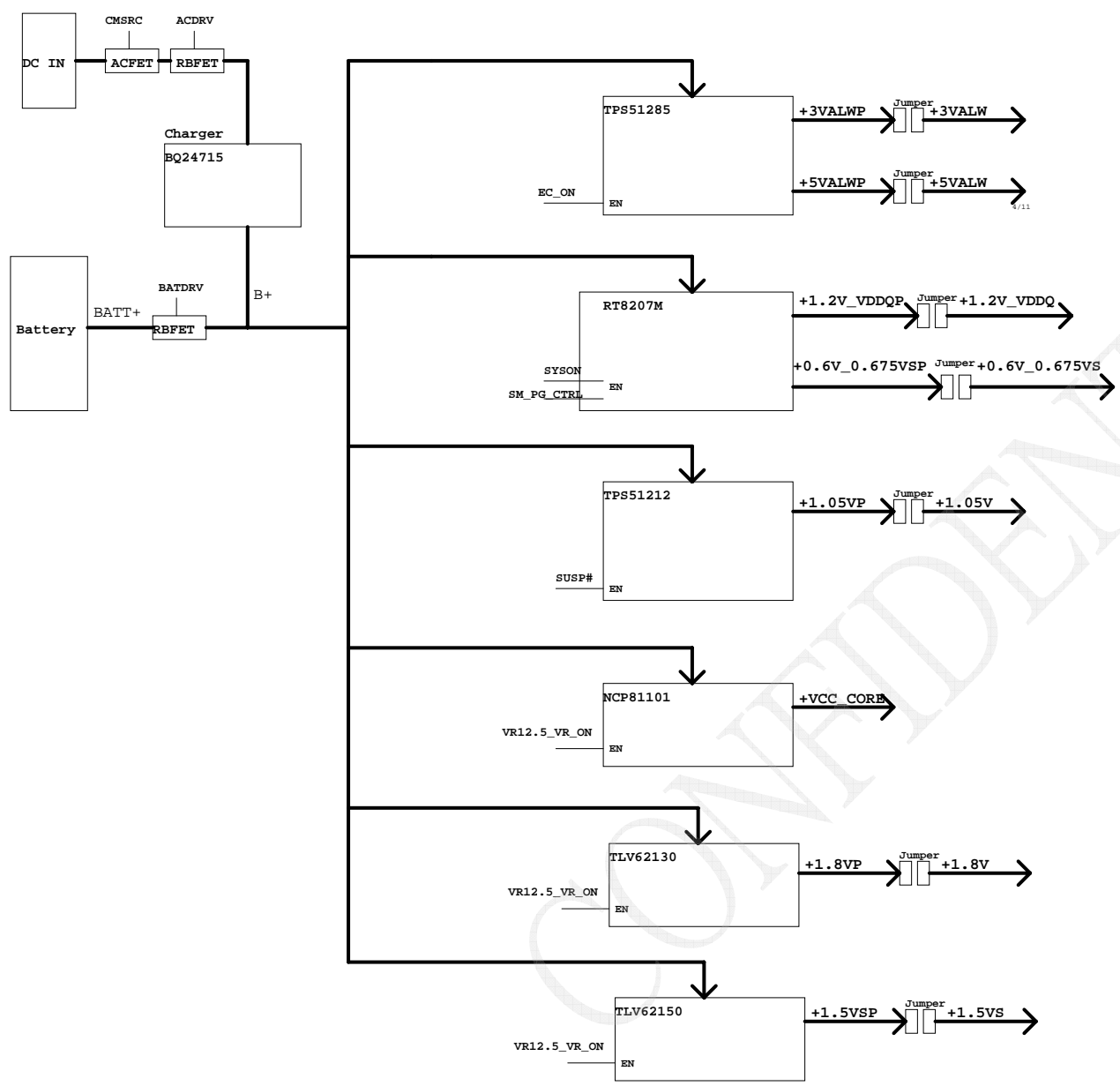
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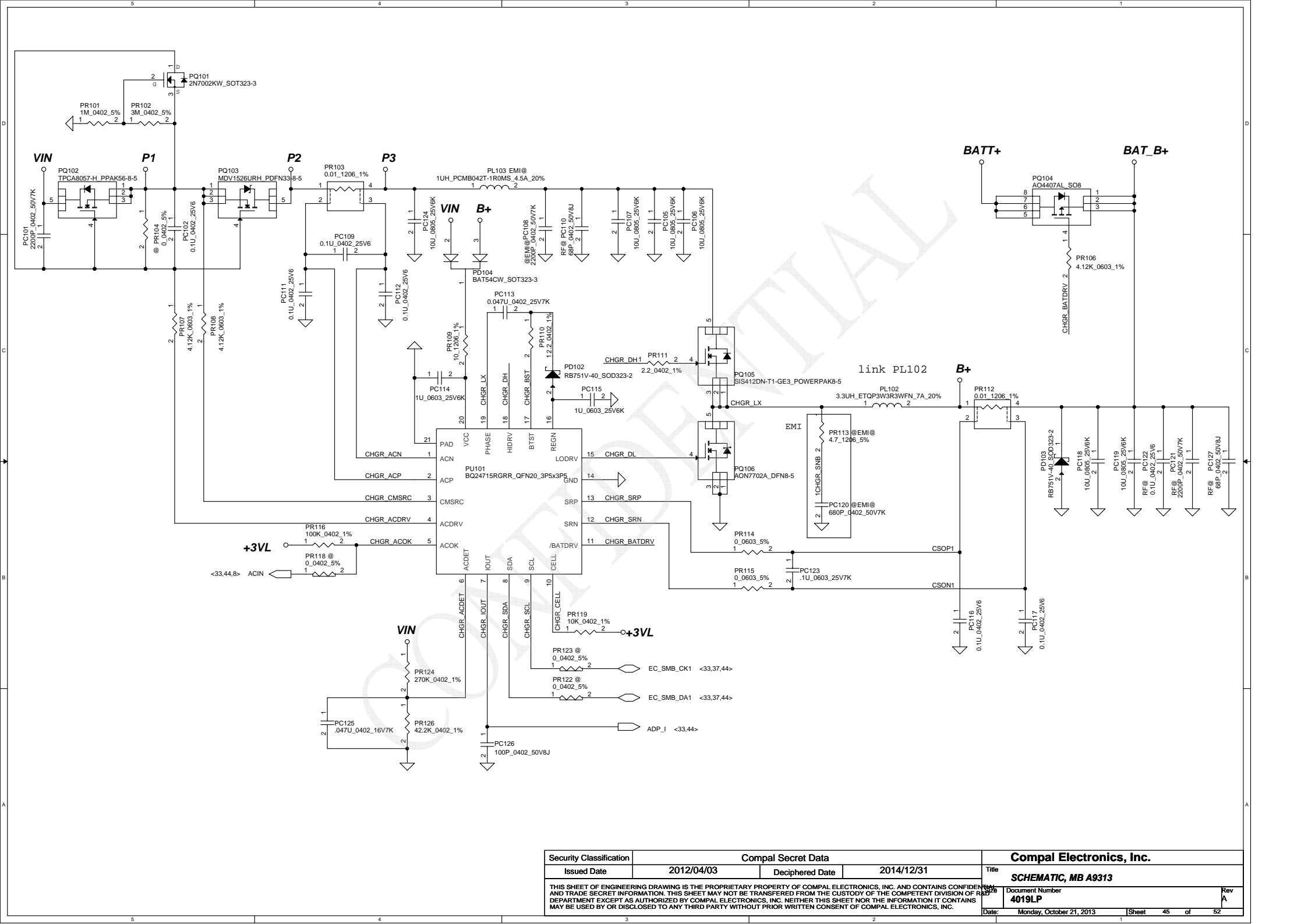
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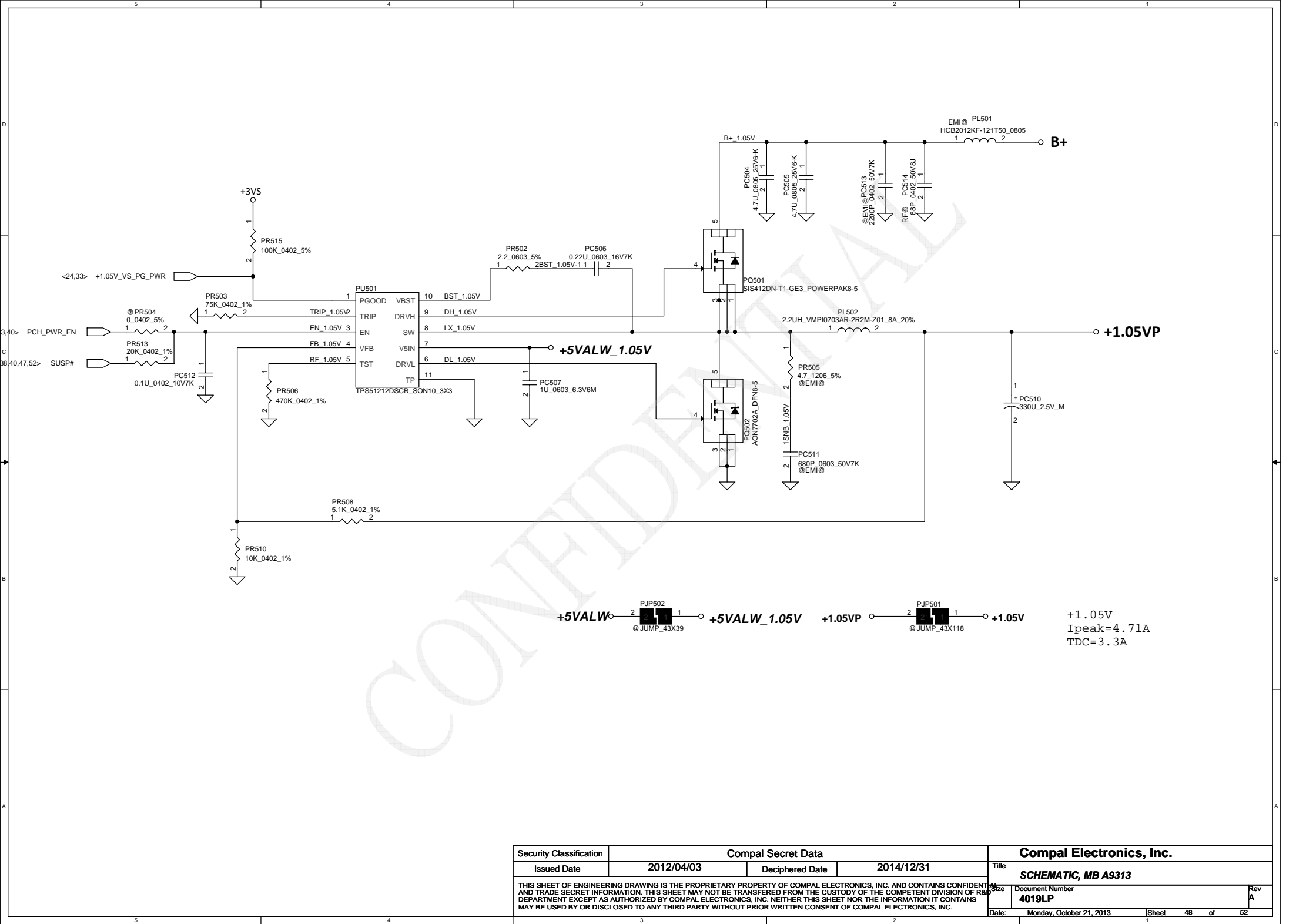




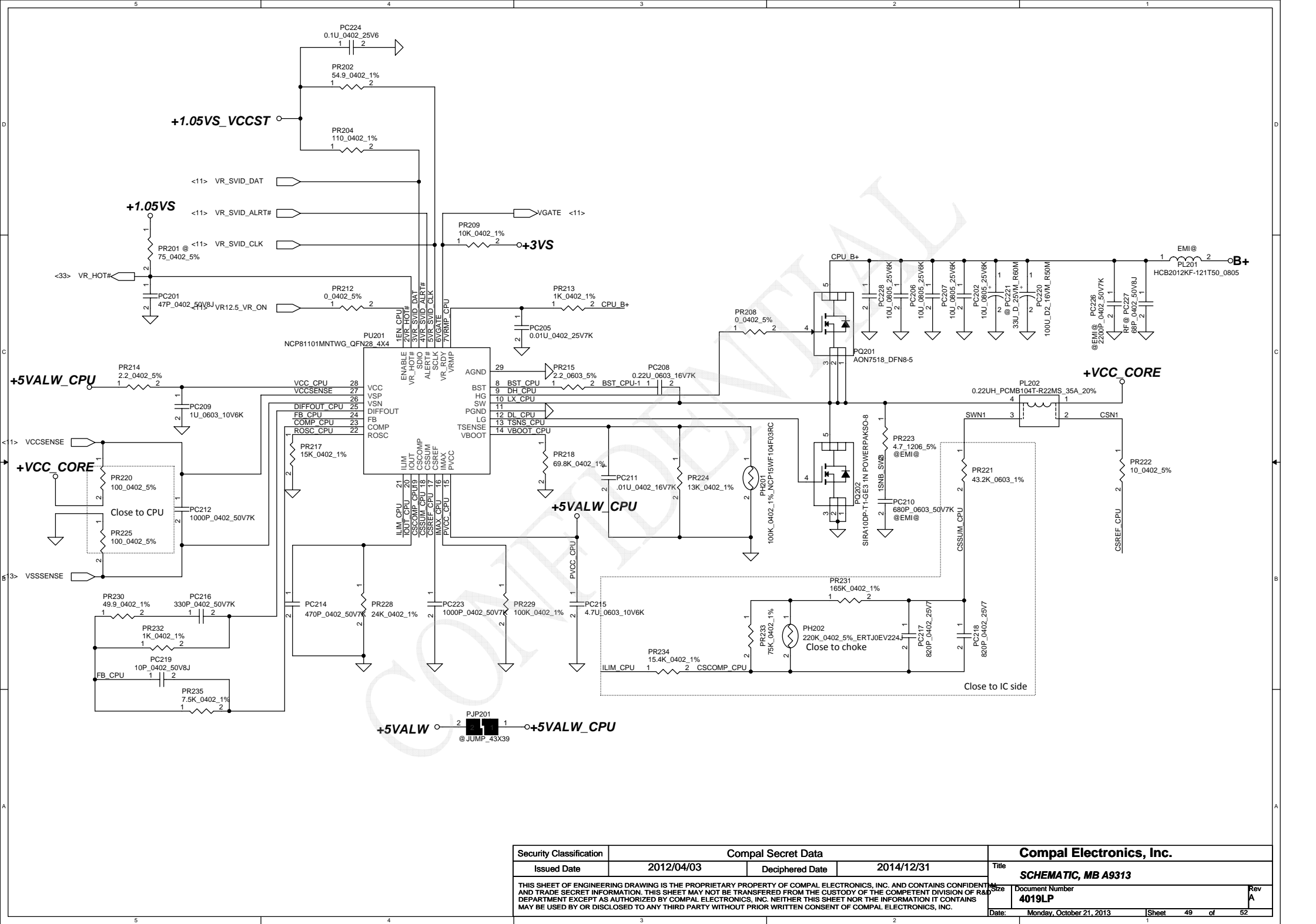
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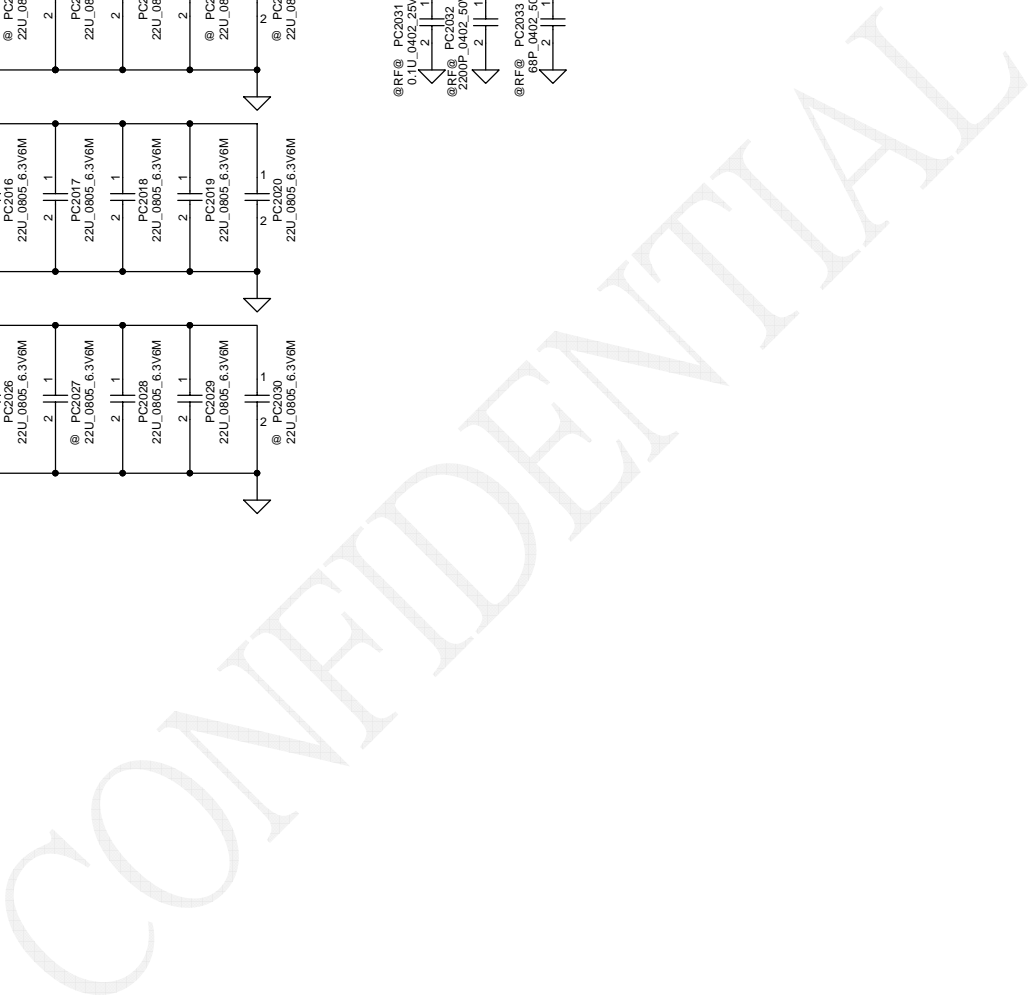






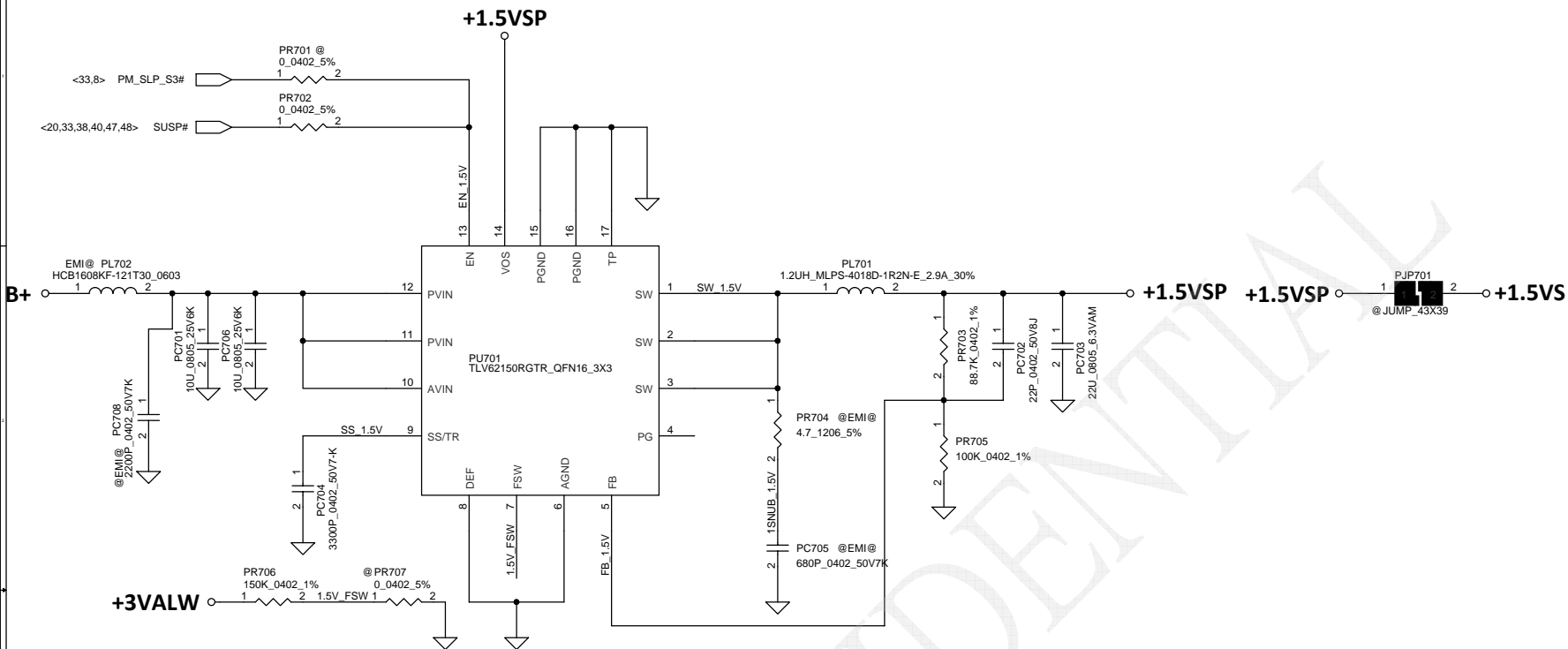






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